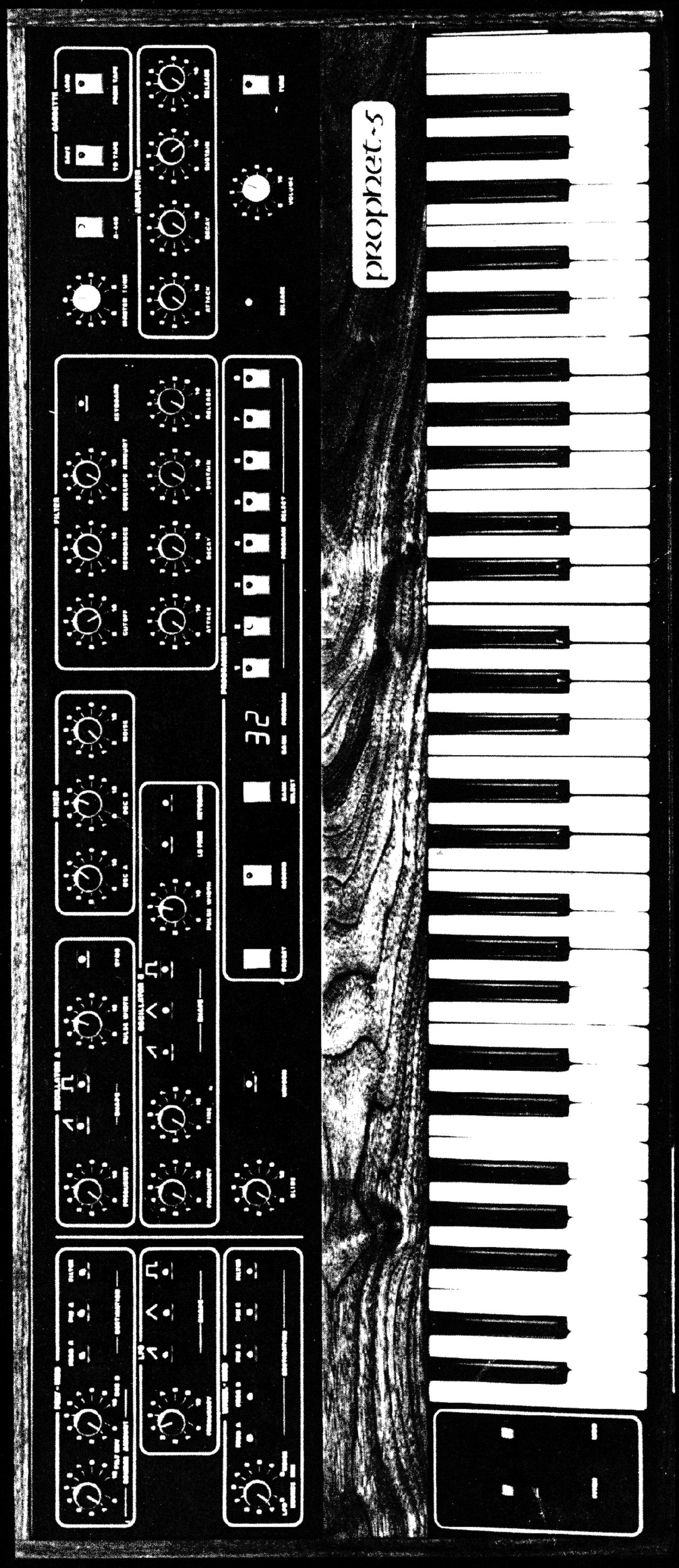


TECHNICAL MANUAL

REVs 3.0, 3.1 & 3.2

SEQUENTIAL CIRCUITS INC

MODEL 1000
S/N 1301 and Above
Revisions 3.0, 3.1 and 3.2
Manual No. TM1000D.2

PROPHET-5 SYNTHESIZER
TECHNICAL MANUAL

SECOND EDITION

By STANLEY JUNGLEIB

PROPHET-5 SYNTHESIZER
TECHNICAL MANUAL

By Stanley Jungleib

Artwork: Denis Simard
Greg Armbruster

Second Edition
For Revisions 3.0, 3.1 and 3.2

Manual No. TM1000D.2
Issued: October, 1981

About This Manual and Servicing The Prophet

The Prophet is a sophisticated instrument and SCI issues its technical manual for use by qualified technicians only. Of course the manual will be read by Prophet owners and others interested in synthesizer design. And we realize it will also be used by some to develop modifications for the instrument. While we support this innovative attitude in spirit, we cannot support it financially: Modifications or unauthorized service void the Prophet's warranty. They also invariably extend service time (thus, cost) if factory repair is required. Familiarize yourself thoroughly with this manual before attempting any work on the Prophet. This will at least help you judge whether you should be working on it at all. If in doubt, please contact our Service Department.

This edition of the Technical Manual (TM1000D) documents Prophet-5s with serial numbers 1301 and above. Although great care was taken to ensure the changes would be transparent to players, technicians will find "Rev 3" quite a different instrument from its predecessors. Rev 2 (S/N 184-1299, see TM1000C) was a mere refinement of Rev 1 (S/N 1-182). Rev 3, however, uses new voltage-controlled ICs in the analog synthesizer and, in the microcomputer, a vastly different ADC, DAC and control voltage distribution scheme. Although the main purpose of the revision was to remove production limitations caused by inconsistent supply and quality of the previous synth "chip set," the hardware redesign encouraged the implementation of more sophisticated editing, tuning and maintenance software while improving servicability; the number of voice trimmers being reduced from 80 to 45.

The manual is organized as follows:

SECTION 1, MECHANICAL provides a physical introduction and directions for disassembling/assembling the Prophet.

SECTION 2, THEORY explains general function and circuit operation, referring to block diagrams and to the schematics for hardware details.

SECTION 3, DOCUMENTS contains schematics and pictorials identifying all components.

SECTION 4, SERVICE contains procedures for routine tests and trims.

SECTION 5, PARTS cross-references component designators to SCI stock numbers.

SECTION 6, GLOSSARY decodes abbreviations appearing on SCI documentation.

SECTION 7, APPENDIX contains selected data sheets.

Your response to the questionnaire on the next page will help us monitor our publication's usefulness.

About The Second Edition

In addition to the original revision 3.0 data (with a few corrections), the following material covering later refinements of the instrument has been added. The revisions occured chiefly in the microcomputer's memory configuration, added PITCH and MOD CV inputs, and in the addition of a serial interface for communication with the Model 1005 Polyphonic Sequencer or Model 1001 Remote Keyboard.

SECTION 8, THEORY discusses the hardware changes comprising revisions 3.1 and 3.2.

SECTION 9, PROGRAMMING covers use of the serial interface.

SECTION 10, DOCUMENTS contains schematics and pictorials for revisions 3.1 and 3.2.

SECTION 11, SERVICE includes instructions for updating a 3.0 or 3.1 instrument to level 3.2, for using the diagnostic memory tests, and for an added adjustment on PCB 3.

SECTION 12, PARTS lists SCI stock numbers for 3.1 and 3.2-level assemblies.

Table of Contents

SECTION 1
MECHANICAL

1-0 GENERAL

This section shows how to remove the Prophet's main assemblies. Not all of the procedures given here should be necessary at any one time. For some service situations you will only need to separate the top and bottom panel assemblies and arrange them as shown in Figure 1-0. This configuration, discussed in paragraph 1-2, allows access to all trimmers on PCB 4 and most trimmers on PCB 3. However, for some PCB 3 trims you will have to swing-out or completely remove PCB 4, as discussed in paragraph 1-3.

1-1 PRECAUTIONS

Observe the following precautions when working on the Prophet:

SWITCH POWER OFF AND CHECK 115/230V SWITCH ON BACK PANEL BEFORE CONNECTING PROPHET TO POWER OUTLET OR AMPLIFIER.

NEVER TOGGLE 115/230V SWITCH WITH POWER ON.

TRIMMING, OF COURSE, MUST BE PERFORMED WITH POWER ON. SO AVOID THE POWER SUPPLY PRIMARY CIRCUITRY, WHICH CONDUCTS LETHAL VOLTAGE.

SWITCH POWER OFF BEFORE DISCONNECTING OR CONNECTING ANY CIRCUITRY, OR REMOVING OR INSTALLING PCBs.

IMPORTANT! WHENEVER THE AUDIO CABLE IS DISCONNECTED, PCB 3 MUST BE GROUNDED TO THE BACK PACK PANEL.

DO NOT BEND OR STRAIN THE PCBs. OTHERWISE MAY CAUSE TINY BREAKS IN THE PRINTED-CIRCUIT TRACES WHICH WILL BE EXTREMELY DIFFICULT TO FIND.

TO REPLACE SOLDERED COMPONENTS SWITCH POWER OFF, REMOVE THE PCB COMPLETELY FROM THE INSTRUMENT AND DESOLDER FROM BOTH SIDES. USE A VACUUM SYRINGE OR DIP DESOLDERER. KEEP VACUUM SYRINGES CLEAN TO PREVENT THEM FROM SPRAYING MOLTEN SOLDER. DON'T OVERHEAT THE PADS. WORK CAREFULLY!

1-2 SERVICE POSITION

TO PREVENT DAMAGE TO THE TOP PANEL, KEYBOARD, OR WOODWORK, USE A CARPETTED OR SIMILARLY-COVERED WORK SURFACE WHEN OPENING THE BOX.

To set up the Prophet for service first switch power off, unplug power cord, and turn instrument over to expose bottom panel. Remove two large screws near front feet. Remove eleven screws around perimeter of bottom panel.

Holding top and bottom panel assemblies together, turn the Prophet right-side-up again. Remove four screws along top edge of back panel. Slowly slide the top panel assembly forward—about nine inches—so when raised the control panel will clear the large power supply capacitors.

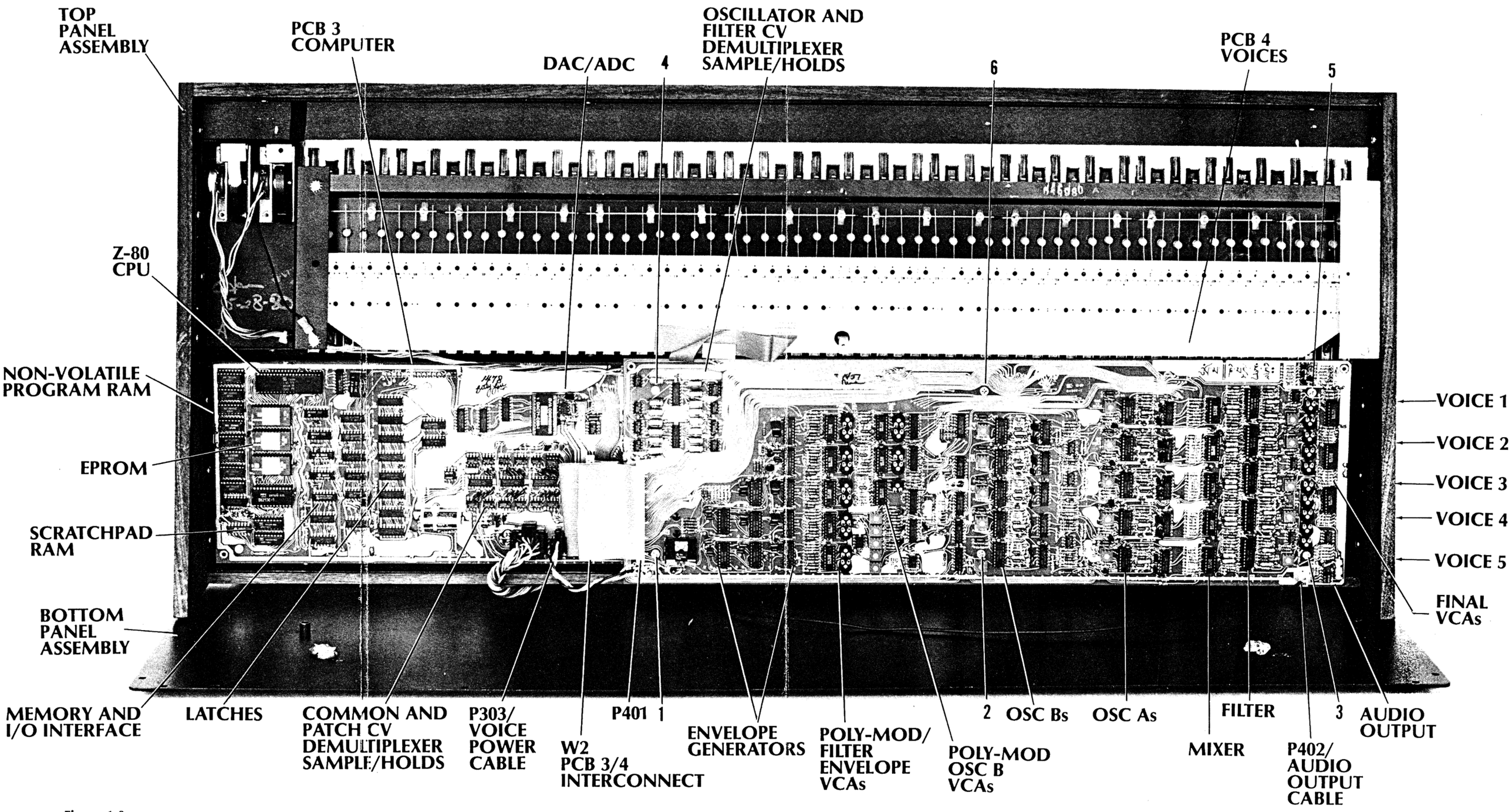


Figure 1-0
SERVICE POSITION

Raise the top panel assembly to service position shown. For best stability both top panel side back edges should rest on the bottom panel. Actually, the top panel upper edge rests on the back panel cable. This is normal; but a small (half-inch) prop may be added to improve stability.

The instrument can operate normally in this position. Of course its operating temperature will be far below normal. This may slightly affect adjustments or the performance of certain ICs.

REMEMBER THAT IN SERVICE POSITION THE TOP PANEL ASSEMBLY BALANCES ON ITS REAR EDGES. DON'T UPSET THIS BALANCE BY PUSHING TOO HARD WHEN PROBING OR TRIMMING.

When reassembling the Prophet, turn instrument over and first start two large screws near front feet. Then start bottom and back panel screws to obtain overall alignment before tightening all screws.

1-3 PCB 4 VOICE BOARD

PCB 4 may be swung-out and operated under power. For this set-up, switch power off, remove screws identified in Figure 1-0 in the order suggested, and position board on insulation as shown in Figure 1-1.

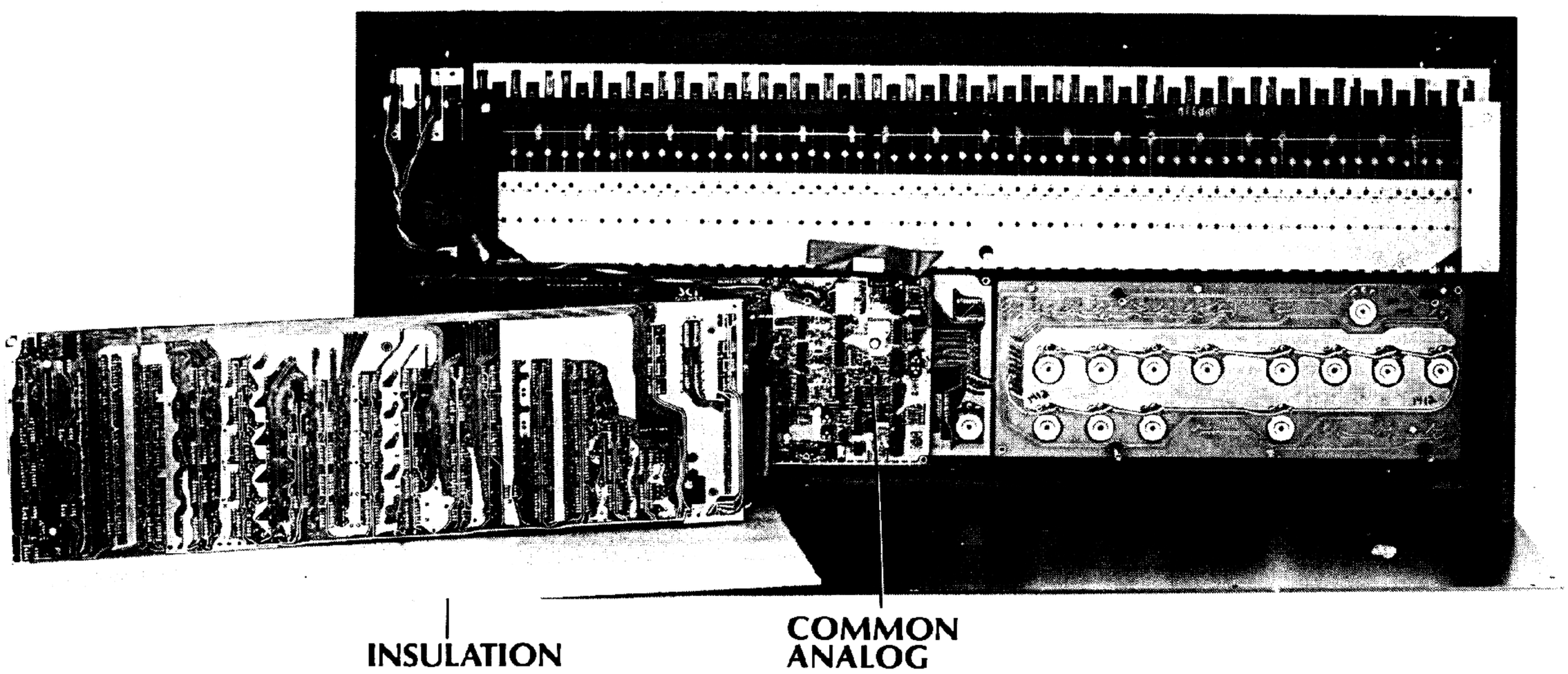


Figure 1-1
PCB 4 SWINGOUT

TO PREVENT GROUND LOOPS, PCB 3 IS GROUNDED ONLY THROUGH THE AUDIO CABLE TO THE BACK PANEL. THEREFORE, WHENEVER THE AUDIO CABLE IS DISCONNECTED, PCB 3 MUST BE TIED TO THE BACK PANEL.

CAREFUL! DON'T ALLOW PCB 4 TO SHORT AGAINST STANDOFFS FROM PCB 3 OR AGAINST THE BOTTOM PANEL.

To remove W2, completely switch power off and disconnect voice power cable at P303 on PCB 3 (see Figure 1-0). Also remove PCB 3/4 interconnect at P401 on PCB4, with a gentle "see-saw" motion. Detach audio output cable from P402.

When reconnecting voice power and audio output cables, be sure tabs interlock. Also be sure the PCB 3/4 interconnect is correctly mated and firmly seated at P304 and P401.

1-4 PCB 3 COMPUTER BOARD

PCB 3 is held by the screws identified in Figure 1-2, and by two direct connectors to PCB 2, behind it. To remove PCB 3 first remove PCB 4. Disconnect back panel cable from P302 and wheel cable from P301, remove screws, and pull while rocking the board to minimize stress.

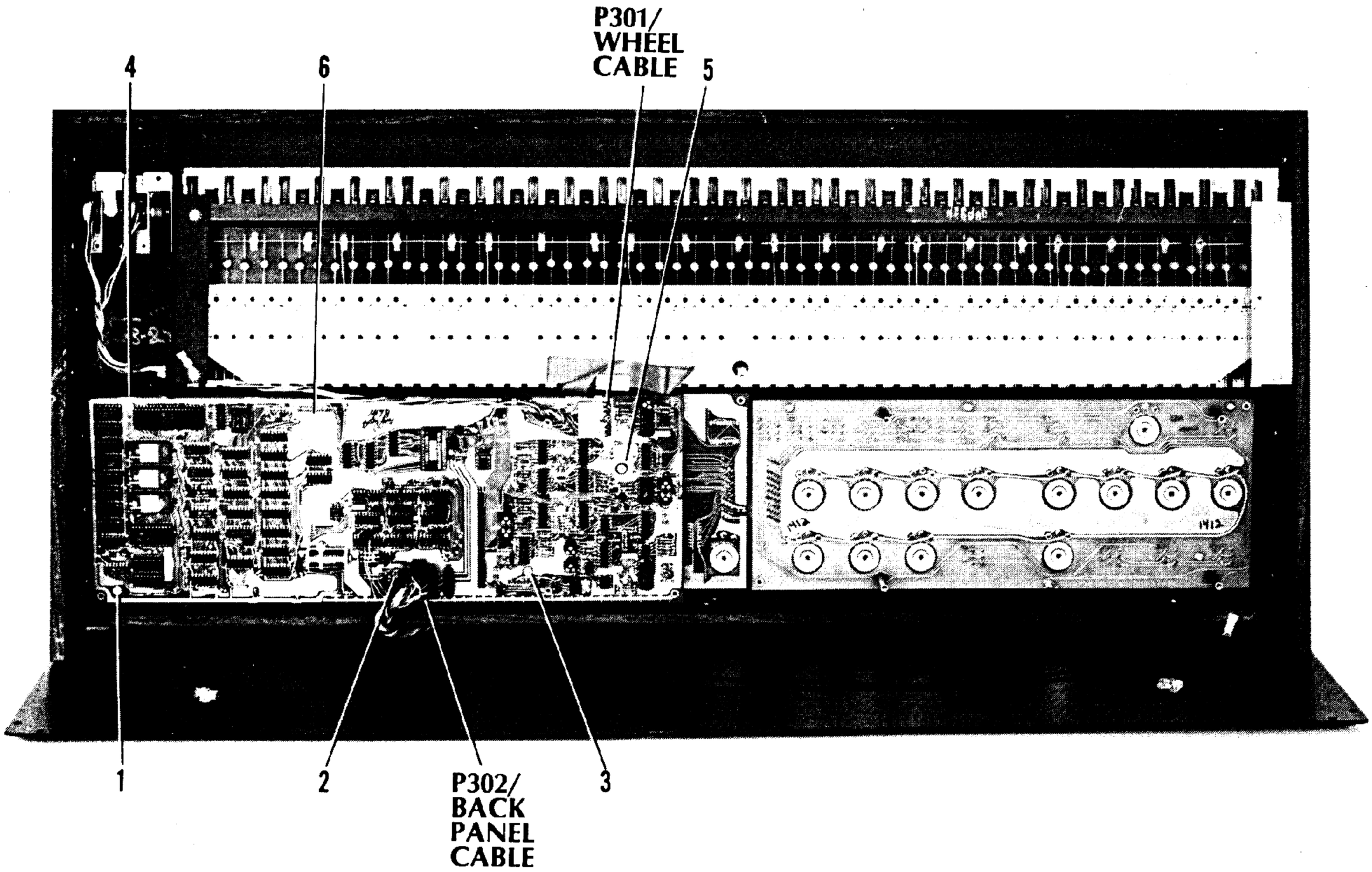


Figure 1-2
PCB 3 MOUNTING

When replacing be sure all connector pins are correctly mated with PCB 2 before fastening screws. Alignment is insured by machine screw holes with their standoffs. Remember to reconnect the wheel cable, too, before replacing PCB 4. When reconnecting wheel and back-panel cables, be sure tabs interlock.

1-5 PCB 1/2 CONTROL PANELS

Once PCB 3 and PCB 4 have been removed, control panel removal involves pulling off all knobs, unscrewing all potentiometer mounting nuts—using a half-inch nutdriver—and removing screws identified in Figure 1-3.

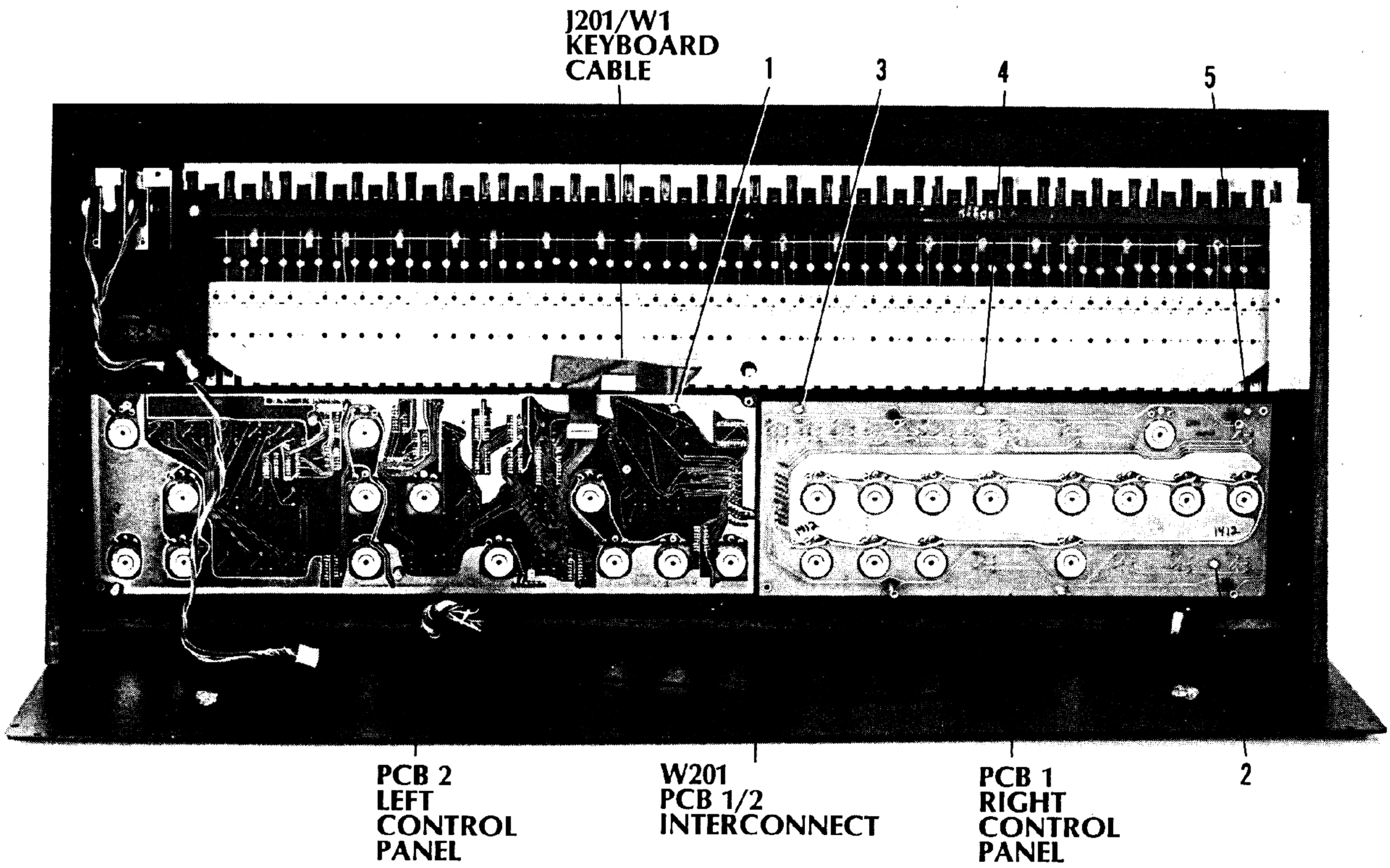


Figure 1-3
PCB 1/2 MOUNTING

When replacing, check keyboard cable, that all pots fit correctly through the front panel, and that switches operate freely before tightening pot nuts.

1-6 KEYBOARD

After removing PCB 3 and PCB 4, turn the top panel assembly over and disconnect keyboard cable at J201 (see Figure 1-3).

Figure 1-4 details keyboard mounting. At both ends, remove keybed supports by first removing keybed screws then rear keyboard mounting screws. Remove front keyboard mounting screws. The entire keyboard will slide out of the case—and back in—as shown in Figure 1-5.

CAREFUL! DURING THIS OPERATION THE J-WIRES FOR THE LOWEST AND HIGHEST KEYS ARE VULNERABLE TO DAMAGE FROM COLLISION WITH THE KEYBOARD MOUNTING BRACKETS. WHEN REPLACING CHECK J-WIRES AT EACH END OF KEYBOARD FOR CONTACT WITH BUS BAR.

Also, remember to attach the wheel ground lug.

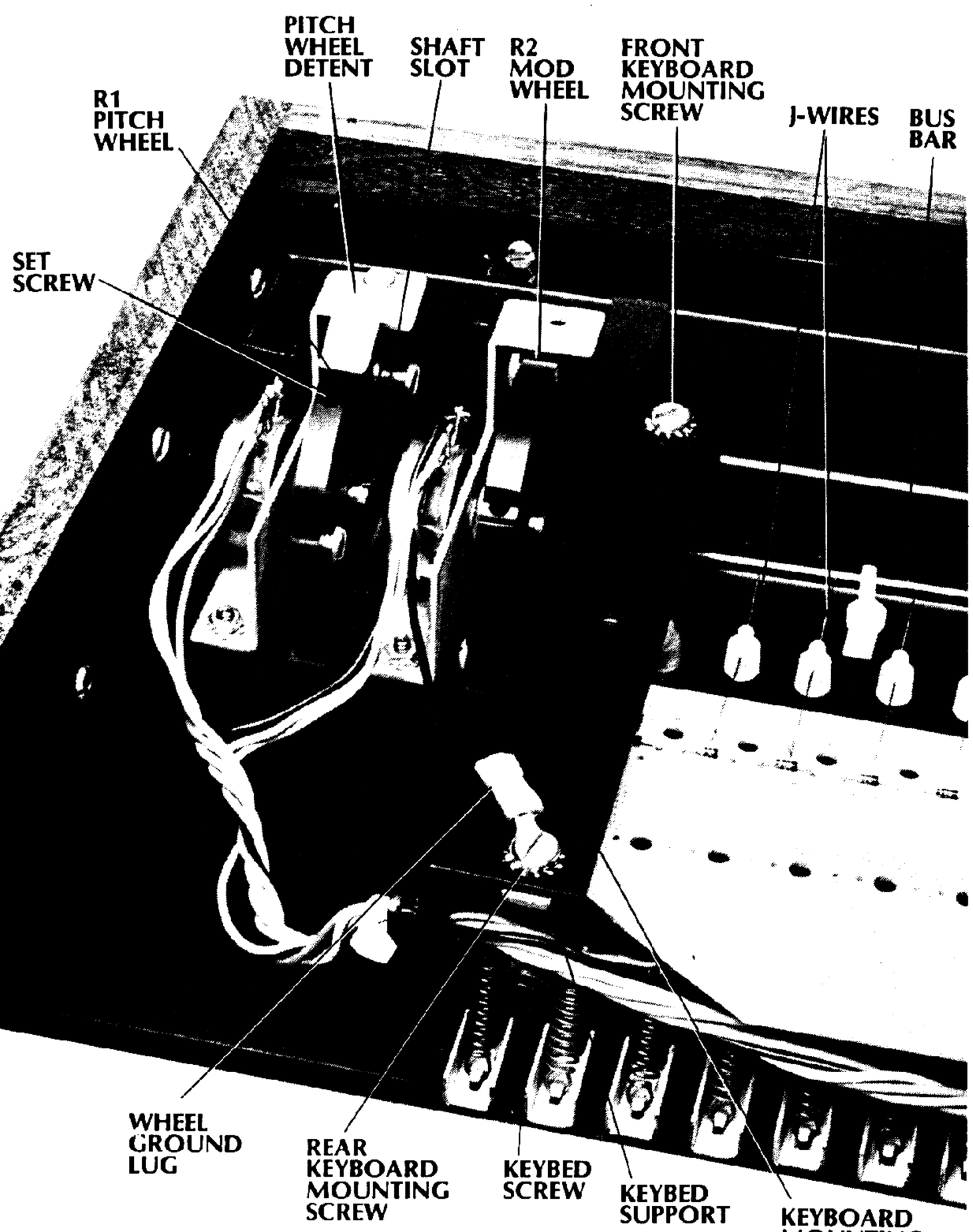


Figure 1-4
KEYBOARD MOUNTING

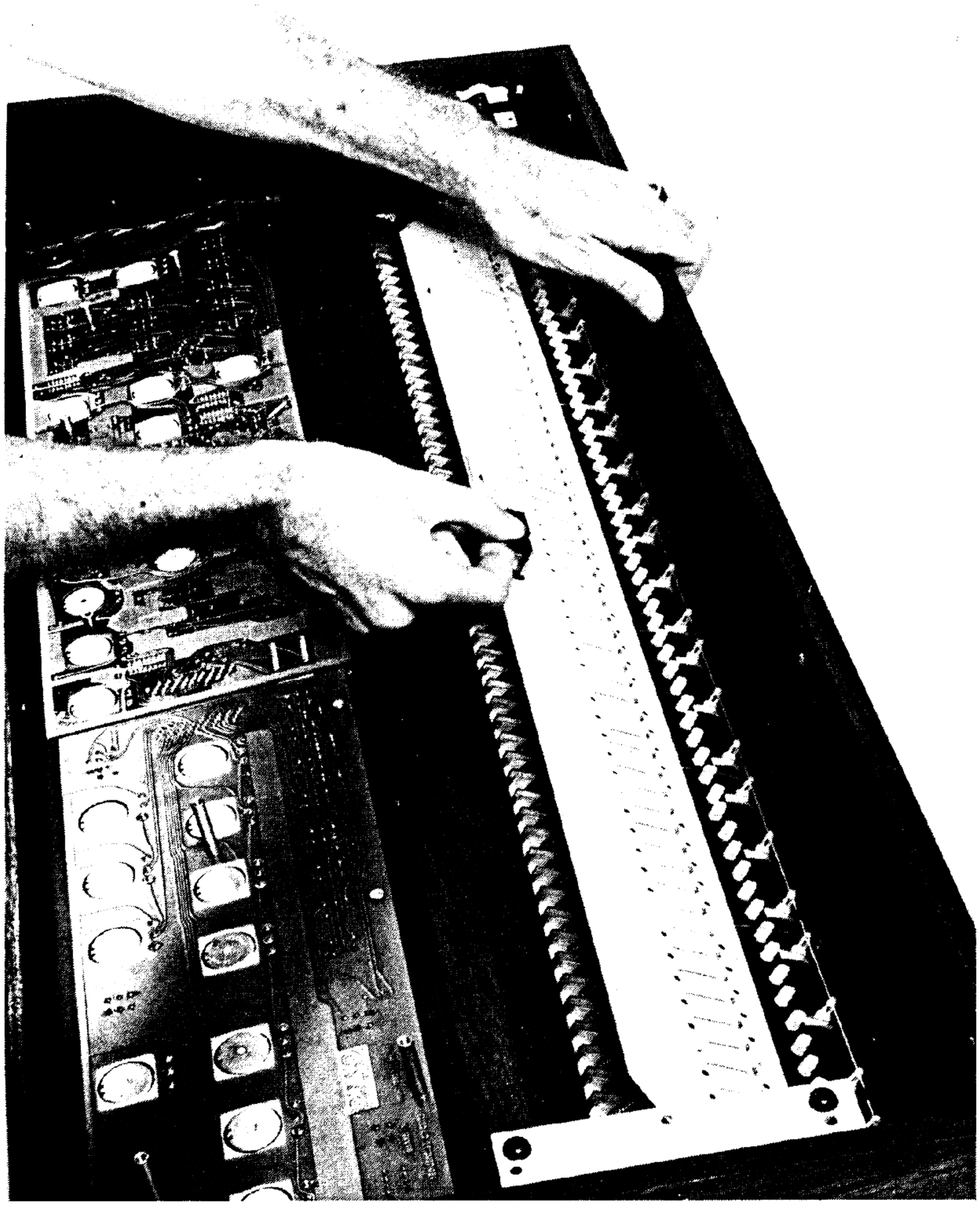


Figure 1-5
KEYBOARD REMOVAL

SECTION 2
THEORY

2-0 GENERAL

This section explains the Prophet's theory of operation. First a general description relates the Prophet to the basic analog synthesizer and introduces the concepts central to the Prophet's advances over conventional performance instruments: programmability and polyphony. Then the analog synth and microcomputer functions are covered and their sub-circuits detailed. Throughout it is assumed the reader is already familiar with Prophet-5 operation (see Operation Manual CM1000B).

2-1 SYNTHESIZER BACKGROUND

The synthesizer is a new instrument but the urge to set technology in search of music is quite old. Consider the pipe organ; of traditional instruments, most like the synthesizer. The organ achieved its broad dynamic, pitch and timbral ranges through intricate mechanical arrays; for generating steady wind, transferring key action to pneumatic valves for each note, activating ranks of pipes, and to couple pedalboards and keyboards. Later, the bellows tremolo and pedal-operated swell shutters were added for dynamic and timbral expression. As the organ expanded into larger halls pneumatic and hydraulic devices were developed to isolate the keyboard from the force required to key more pipes at higher wind pressure. With the advent of electricity the keyboard and drawknobs, formerly levers, became switches. Elaborate relay banks now drove solenoid valves for each pipe. More recently, electronic organs—in many variations—have relied on motor-driven tone generators or switch/relay banks for oscillator frequency division or waveform addition or shaping. Another influential technology, the tape recorder captured natural, instrumental, and electronic sounds for new uses and stimulated the idea of composing music not performable "in real time" on conventional instruments. A few keyboard instruments have been directly based on tape mechanisms.

Now, what is a synthesizer? It can be distinguished from the organ or tape recorder by reliance on electronic rather than mechanical devices to generate and modify sound. Except for performer's controls a synth need have no moving parts. (Even this exception may one day disappear.) Thus it is far more flexible and controllable than an organ. In contrast to organ or tape technology, voltage control (VC) allows the immediate and precise adjustment of the basic parameters of an audio stage such as oscillator (VCO) or filter (VCF) frequency, or amplifier (VCA) gain, by a signal from another VCO, an envelope generator (ENV GEN), keyboard (KBD) or sequencer (SEQ). Most music is analyzable into elements replicable by a few VC-modules. For example, if a synth imitates a drum or piano it is not by being a (mechanical) percussion instrument, but by simulating the dynamic envelope accompanying percussive sounds with a VCA under control of an ENV GEN.

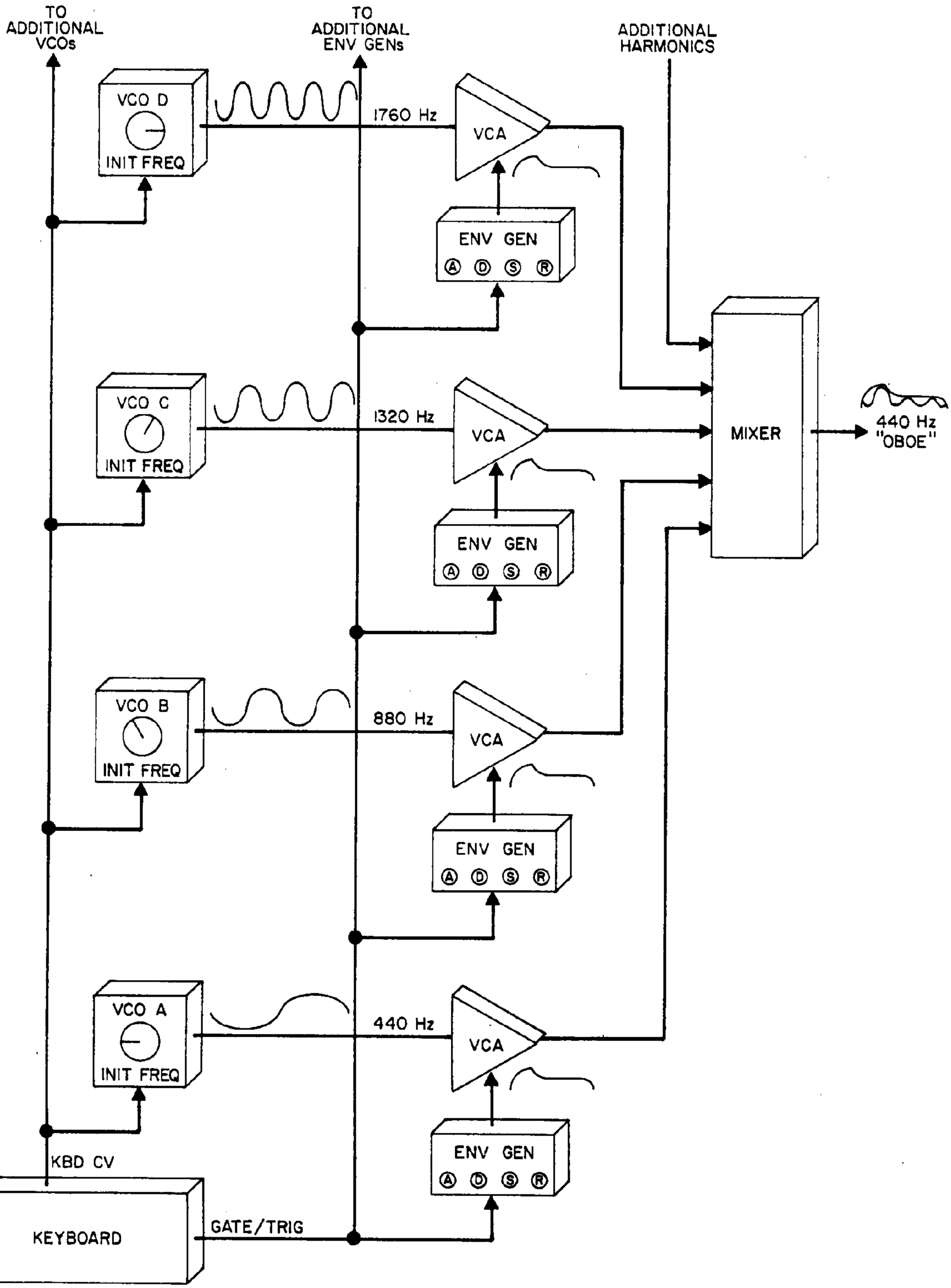


Figure 2-0
MONOPHONIC ADDITIVE SYNTHESIS

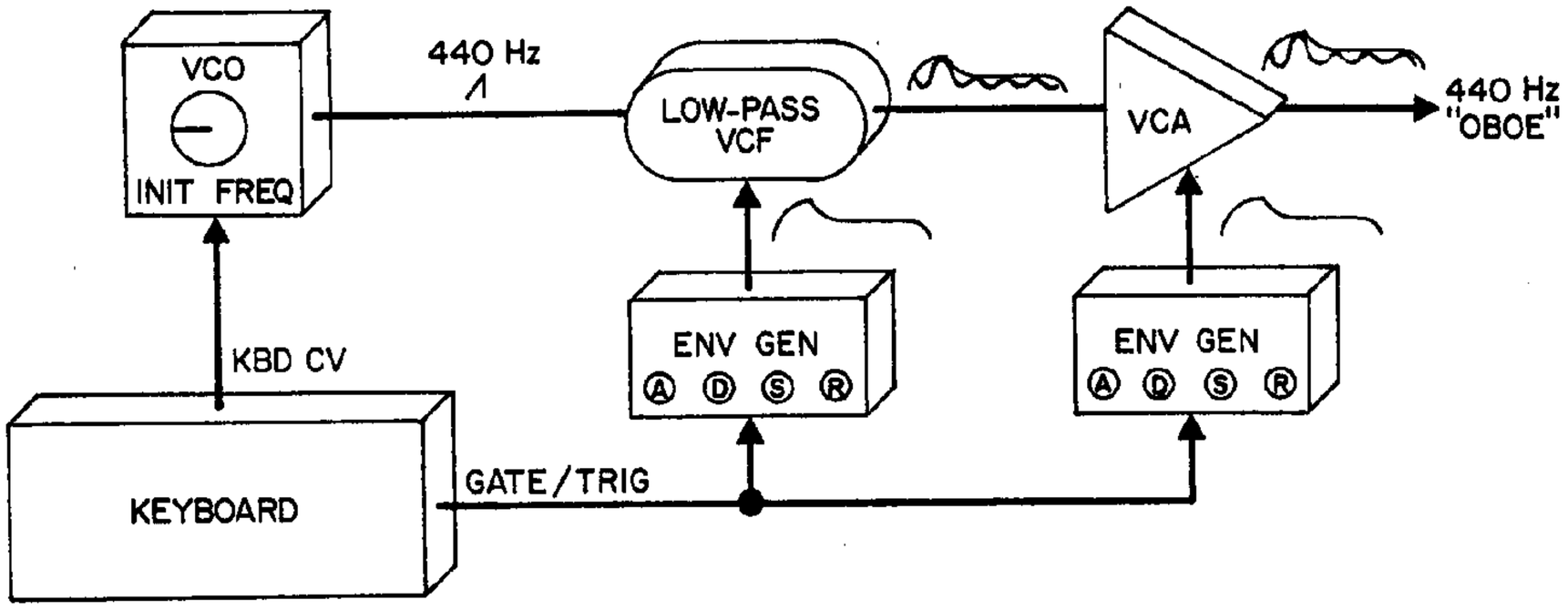


Figure 2-1
MONOPHONIC SUBTRACTIVE SYNTHESIS

Besides a dynamic envelope a musical voice usually has a pitch and timbre which consists of a fundamental and a number of harmonic frequencies—all of varying relative strengths. Pitch and timbre synthesis raises a distinction between two techniques, diagrammed in Figures 2-0 and 2-1. The first technique, additive synthesis, might create a timbre by summing the output of several sine-wave VCOs for the fundamental and each harmonic. In contrast, subtractive synthesis can start with one sawtooth-wave VCO generating the fundamental with extensive harmonics, then obtain the desired timbre by subtracting unwanted harmonics with a low-pass VCF.

The additive and subtractive techniques have encouraged the development of two types of instruments, roughly, "studio" and "performance." Actually most organs use additive synthesis, but since with a synth one can individually control the level of each harmonic over time additive synthesis may be potentially more accurate for synthesizing a particular sound. Whether additive or subtractive, studio synths may be configured from dozens of modules interconnected by patch cords. The modules have knobs to establish the initial settings of VC-parameters such as initial frequency (FREQ), pulse width (PW), and resonance (RES). But the flexibility and complexity of modular synths has discouraged their live use on stage because significant sound changes often require repatching modules and precisely checking knobs. Favorite, complex sounds take a long-time to create, and almost as long to recreate on a modular synth. So these monophonic (one-voice) synths instead feed multi-track recorders on which polyphonic interpretations or compositions are actually orchestrated.

A comparison of the number of modules and interconnections depicted in Figures 2-0 and 2-1 shows why the subtractive configuration has become the popular technique for performance synths. Subtractive synths may be smaller, so, more portable. Their patches will not be as elaborate, so, easier to change. Originally, performance synths were monophonic. Or they exploited organ technology so more than one note could be played at a time. "Preset" switches that select fixed patches supplanted many modular controls. Though one could certainly change sounds quickly by using them, many players have found preset synths unsatisfactory because they eliminate an essential part of synth musicianship—control of the sound itself. Some manufacturers have offered partially-programmable instruments. But before the Prophet appeared it was not possible for a keyboardist to instantly select his or her own customized synth sounds and play them polyphonically.

2-2 THE PROPHET

The Prophet is a subtractive, analog synthesizer suitable for performance or studio use. It provides instantaneous patch repeatability and polyphonic capability without the limitations of organ technology or fixed presets. The term "digital-analog hybrid" is often used to describe the Prophet. It means the digital computer controls the analog audio sources and modifiers. The computer itself generates no sound (except for the A-440 reference).

Figure 2-2 diagrams the Prophet at the most general level. Instead of controlling the synth directly, the keyboard and most controls are processed through a microcomputer system. The system provides a way to store all of the switch and knob settings which form a patch, and solves the problem of generating five sets of oscillator (OSC) and filter (FILT) CVs and GATEs from a single keyboard. The Common Analog circuitry mixes the few non-processed controls with processed signals for the voices. Although only one voice is depicted on the control panel, the black knobs and switches patch the five voices identically. This makes the voices homophonous—they sound alike—with pitch differences corresponding to (at most) five simultaneously-held keys.

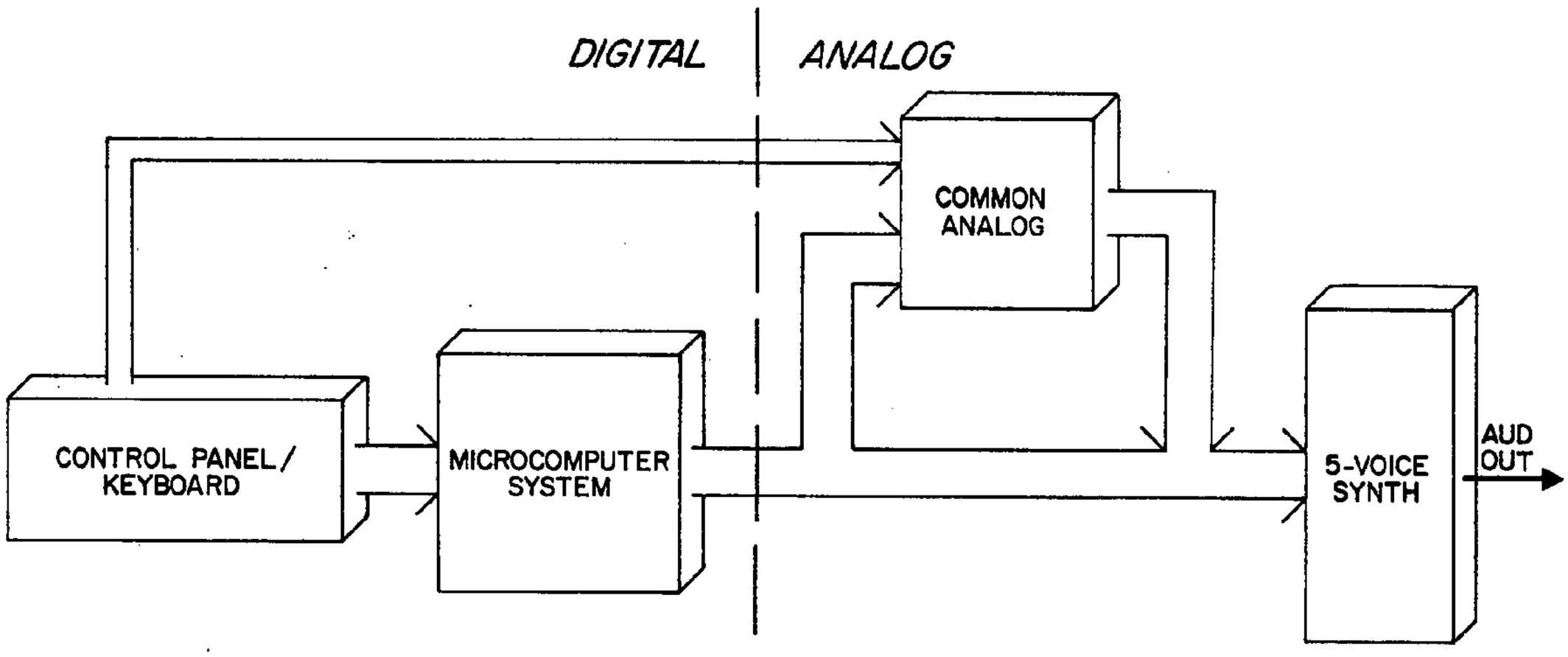


Figure 2-2
PROPHET GENERAL BLOCK DIAGRAM

Figure 2-3 shows the principle functions of the four main blocks. Beginning with AUDIO OUT, the voice outputs are combined and overall volume set by the VOL VCA controlled directly from the control panel. Each voice is a complete synthesizer with two VCOs, a MIXER, VCF, FINAL VCA, and two ENV GENs. Each of the ten VCOs has its own FREQ CV, which allows the computer to individually fine-tune them and allows the voices to follow separate keys. Each voice receives its own GATE, which triggers the two envelope generators with each keystroke.

All switch commands and most CVs are generated by the computer. Non-processed CVs include MASTER TUNE, PITCH-bend, and WHEEL-MODulation which are mixed in the Common Analog circuitry. The Common Analog circuitry also requires a few switch commands.

The microcomputer performs the task of voice assignment. It decides which held keys sound which voices through the OSC and FILT CVs and GATEs. Voice 1 is assigned to the first key hit, Voice 2 to the second key, and so on. After the five initial assignments the system is "last note priority." The earliest-used voice is reassigned to each new note played. Repeated notes key the same voice. For example, holding C, D, E, F, and G, sustains Voices 1, 2, 3, 4, 5, respectively. Adding A "steals" Voice 1 from the C-key, whose pitch disappears even though the key may still be held.

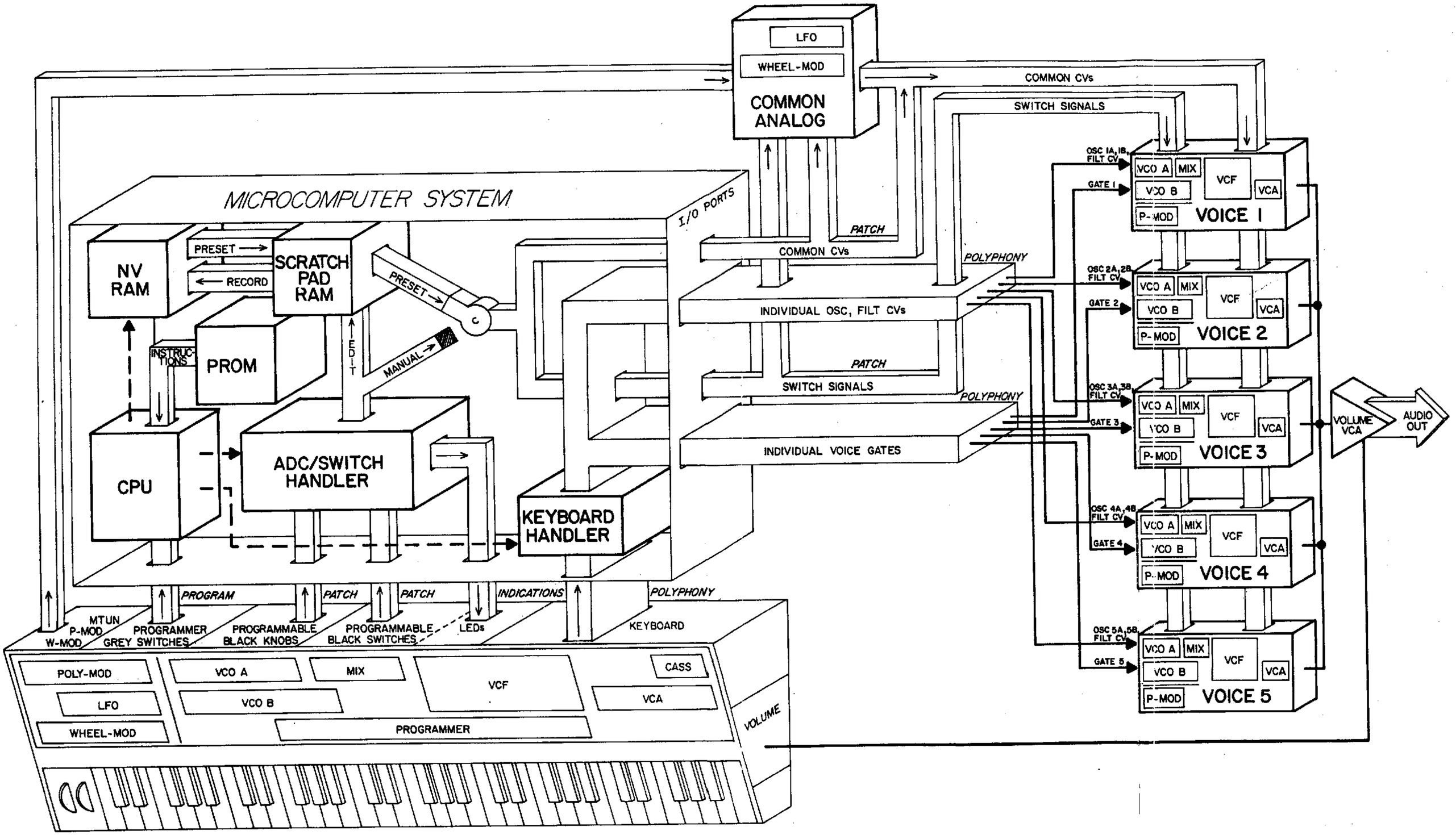


Figure 2-3
PROPHET FUNCTIONAL BLOCK DIAGRAM

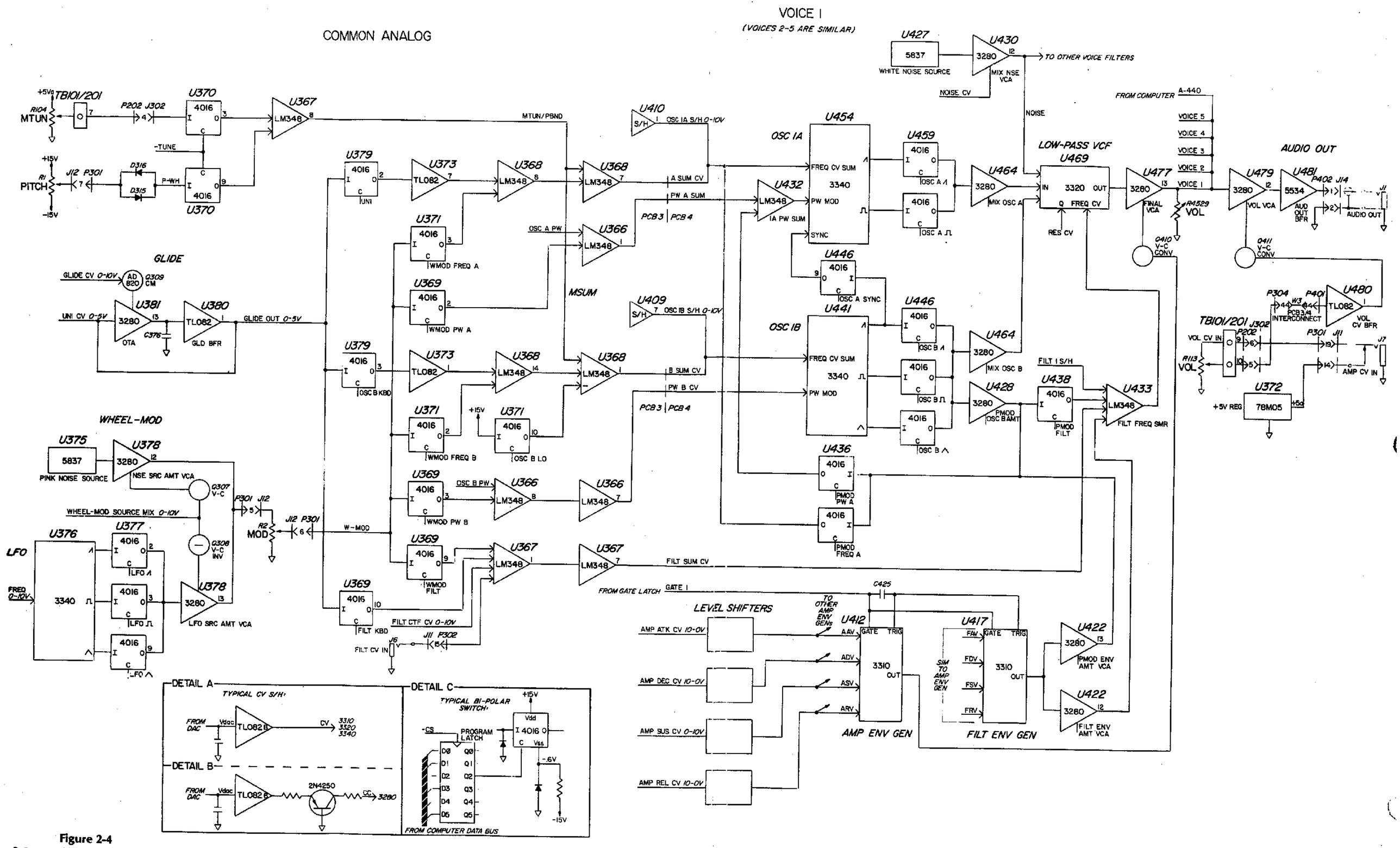


Figure 2-4
ANALOG SYNTH ABSTRACT SCHEMATIC

In UNISON (monophonic) mode a UNISON CV derived from the lowest note played on the keyboard becomes the main pitch control for all voices through the Common Analog circuitry. The five GATEs occur simultaneously, but the envelope generators only re-trigger if no keys are held.

The microcomputer system itself consists of the microprocessor or CPU, memory (MEM), and input/output (I/O) interface. The CPU executes the program permanently residing in the read-only memory (EPROM). This program determines how the various input devices—keyboards, switches, and knobs—are "read", and how "data" generated by them is "processed" to control the synthesizer. The Scratchpad RAM is the CPU's work area. It holds data representing the current status of the keyboard and all controls. Control status depends on the operational mode. In MANUAL mode the control data corresponds to the current settings of the black, programmable knobs and switches. If desired this data can be recorded from Scratchpad to the Non-Volatile Memory (NV RAM). Then, in PRESET mode, selecting recorded programs moves them from NV to Scratchpad, reprogramming the synthesizer for that sound. The EDIT feature allows one to alter individual control settings in Scratchpad, which can then be recorded to supplement or replace the original program in NV RAM.

The remainder of this section discusses the Prophet's actual analog and microcomputer circuitry. Each sub-circuit is described functionally in relation to its block diagram. Principal ICs and any uncommon designs are explained. However the function of common linear, TTL, and MOS ICs is not covered because anyone contemplating technical work on the Prophet must already be familiar with, for example, combinational logic and op amp circuits.

2-3 ANALOG SYNTHESIZER DESCRIPTION

The definitions of the various CV and switch commands in the analog synthesizer must be clear before the Voice and Common Analog sub-circuits can be discussed. Referring to Figure 2-4, the Common Analog circuitry includes the master summers (MSUMs), Glide, and WHEEL-MOD circuits. The MSUMS produce five Common Analog output CVs: A SUM, B SUM, PW A SUM, PW B SUM, and FILT SUM CV. These enable simultaneous pitch control and modulation for the voices, as follows.

R104 MASTER TUNE (MTUN) and R1 PITCH wheel adjust OSC A and B frequency directly—that is, without computer processing—through A SUM CV and B SUM CV. To prevent interference with the TUNE routine (see paragraph 2-13), the switches shown disconnect these controls during the TUNE routine. In UNISON mode the KBD component of the FREQ CV appears through the UNISON CV. The OSC B KBD and FILT KBD switches are for keyboard tracking in UNISON mode. UNISON CV is processed through the Glide circuit which, essentially, delays quick changes in UNISON CV as GLIDE CV increases. The OSC B MSUM is similar to OSC A. FILT SUM CV mainly consists of the FILT CTF CV (which follows the FILT CUTOFF KNOB). An external FILT CV IN can be added through the back panel.

The W-MOD signal, switchable to any MSUM consists of pink noise or LFO output as determined by the W-MOD SOURCE MIX CV. CV inversion to the LFO VCA allows the NOISE and LFO levels to move in opposite directions for a single CV. The MOD wheel sets this mixture's output level to selected MSUMs.

Besides the Common Analog output CVs there are two types of computer-output CVs which terminate at the voices. First, Patch CVs control all five voices identically. For example, all five Amplifier Envelope Generator attack times will be equal for any patch, so the Amplifier Envelope Generator ATK CV is wired to the same terminal on all five AMP ENV GENs. Other Patch CVs include MIX OSC A, P-MOD ENV AMT, and FILT RESONANCE. Second, the Individual CVs determine the frequency of a single VCO or VCF alone. Each voice has two OSC S/H CVs and one FILT S/H CV. These signals contain the polyphonic KBD component of the total FREQ CV applied to these devices. The ten OSC S/H CVs also contain INIT FREQ control—actually common to the OSC As or Bs—and the TUNE "biases", which fine-tune each VCO.

All processed CVs originate from the computer at a separate Sample/Hold (S/H). This circuit is discussed in paragraph 2-12, but for introduction Figure 2-4, Detail A shows a typical S/H used with VC-devices. Detail B adds a voltage-to-current converter (V-C CONV) required to control the operational transconductance amplifiers (OTAs—see paragraph 2-5) used as "VCAs" in all places. Twenty-three S/Hs on PCB 3 supply the Common Analog and Patch CVs and fifteen S/Hs on PCB 4 supply the Individual OSC and FILT CVs.

Voice 1 is used for explanatory purposes, below. The five voices are functionally identical. See schematics SD431 and SD334.

2-4 OSCILLATOR A, B, AND LFO

The Prophet's eleven oscillators—two per voice, plus one LFO—are based on the CEM 3340 integrated VCO. The IC is scaled at 1V/octave. This means an overall CV change of exactly 1V ideally produces a pitch change of exactly one octave. So a CV change of 1/12V (83.3 mV) changes pitch by one semitone. In the voices the basic oscillator range is nine octaves; resulting from 0-5V supplied by the KBD and 0-4V supplied by the OSC FREQ knob through the OSC S/H CV (see Figure 2-4). While most CVs in the Prophet are quantized by only the most significant seven bits of a fourteen-bit DAC into 128 83.3-mV steps (128 x 0.0833V = 10.67V), the OSC S/H CVs are quantized by the full fourteen bits into 16,384 651-uV steps (16,384 x 0.000651 = 10.67). This finer resolution allows the TUNE circuitry to tune the oscillators to within 1/128 semitone. It also allows the SCALE MODE feature, where each note can be raised or lowered by up to a semitone. (For further information, see under DAC and TUNE, paragraphs 2-12 and 2-13). In UNISON mode the KBD CV is routed through the Glide circuit and the OSC MSUMs.

Additional OSC 1A FREQ control is created on Voice 1 itself through the POLY-MOD circuit. The P-MOD FREQ A switch applies a CV mixed from the P-MOD FILT ENV and P-MOD OSC B AMT VCAs to the OSC 1A CV SUM input. OSC 1A's pulse width is controlled by two CVs at the OSC A PW SUM. First PW A SUM CV originates in the Common Analog circuitry as the sum of OSC A PW and W-MOD PW A (if ON). Second, the P-MOD PW A switch can add a CV mixed from the FILT ENV GEN and/or OSC B. When on, the OSC A SYNC switch tunes OSC A to harmonic frequencies of OSC B or changes OSC A's timbre when the two are not in harmonic relation. This occurs independently of whatever OSC B waveforms are switched on.

OSC B is similar to OSC A except that besides being a pitch source it can be a modulation source through POLY-MOD, and can operate as an LFO with or without KBD control. In the OSC B MSUM, the OSC B LO FREQ switch adds a -7.5V offset through B SUM CV. To provide adequate control range, the INIT FREQ control doubles its range (to 9V) when OSC B LO FREQ is ON.

The LFO itself is not controlled by the keyboard, and its pulse width is fixed at 50% (square wave). Its output is a modulation CV effective through the five MSUMs.

Details of the 3340 and associated components can be found on its Data Sheet in the Appendix. All 3340 outputs are positive-going. But using the LFO and OSC B as a modulation source requires their triangle peaks travel as far negative as positive for smooth vibrato. On Voice 1, circuitry containing U451-1 (see SD431) shifts down the dc-level of the triangle to be symmetrical about ground.

While creating a symmetrical signal for modulation, the triangle level-shifting poses a slight problem for the 4016, which is basically designed to pass only positive voltages. Figure 2-4, Detail C shows the basic circuit used for switching all bipolar signals in the Prophet. Instead of being grounded, the Vss pin is biased slightly-negative, allowing the switch to pass slightly negative voltages. Diodes at each switch input protect the switch by clamping negative voltages to not exceed the diode drop, which is also the negative bias value (0.6V). Where a bipolar voltage (such as P-MOD OSC B with OSC B TRIANGLE on) is being switched, the level must be sharply attenuated. where a current (such as all summing nodes) is being switched, the only voltage developed is by the 4016's ON resistance (300 ohm, typical) since the op amp node following the switch is a virtual ground.

2-5 MIXER AND AMOUNT VCAs

The Mixer on each voice sets the level of selected OSC A or B waveforms sent to the filter. Noise level is set in one place for all voices. All of the Prophet's VCA circuits use the RCA 3280 dual operational transconductance amplifier (OTA). The OTA is similar to the typical op amp in input and open-loop gain characteristics but the output is current rather than voltage. (So there must be a load to develop any significant voltage.) The magnitude of the output current is equal to the product of the transconductance (rather than the voltage gain) and the input voltage. The transconductance is adjusted by the amplifier bias current (Iabc) at pins 3 and 6 (see Appendix). A second terminal, Id at pins 1 and 8 control the transfer characteristic (as shown on Data Sheet). In effect, Id controls the input impedance of the OTA. For example, with Id cut off, as at U464-1 MIX OSC A, U464-8 MIX OSC B and U428-1 P-MOD OSC B, Zin ranges 100 Kohm. With Id active, as at U477-1 FINAL VCA, U422-1 P-MOD ENV and U422-8 FILT ENV, Zin ranges 600 ohm.

Since the 3280 is controlled by current, the term CV is not accurate in this context. All 3280 "CVs" are converted to control currents by a 2N4250 PNP transistor as shown in Figure 2-4, Detail B.

In most places, BALANCE trimmers cancel OTA dc-offset, ensuring that even with maximum Iabc, there is no output with no input signal.

The OTA is the central component in the Glide circuit, which also contains current mirror Q309 and voltage follower U380-1. GLIDE OUT CV is fed back to the OTA input so positive or negative current will flow if there is a difference between it and UNISON CV. When GLIDE CV is 0, Iabc will be maximum because the diode-connected current source biases the other transistor's emitter 0.6V above ground. Transconductance will therefore be maximum, so plenty of current is available to charge C376 and GLIDE OUT CV will follow UNISON CV very closely. However as GLIDE CV increases, Iabc decreases, reducing the rate of charge to C376. It will thus take longer for GLIDE OUT CV to approach UNISON CV. This creates a slew between the discrete voltage steps of the input UNISON CV.

2-6 FILTER

The Prophet's five low-pass filters are based on the CEM 3320 integrated VCF. Its scale matches the VCO scale of 1V/OCT, so is also adjusted in semitones by 83-mV DAC steps. Filter frequency is controlled by three CVs summed by U433-7 FILT FREQ SUM. FILT 1 S/H is the Individual CV, FILT SUM CV is the Common Analog output, and the P-MOD FILT switch can add a POLY-MOD CV. R4133 adjusts the FILT FREQ SUM gain.

Details of the 3320 and associated components can be found on its Data Sheet in the Appendix.

2-7 ENVELOPE GENERATORS

The FILT and AMP ENV GENs are based on the CEM 3310. Its output is a positive dc-voltage whose level changes over the time periods set by the input timing CVs. When applied to the VCF and FINAL VCA, the transient voltage determines the frequency and amplitude contours of the voice.

FILT ENV GEN output to the FILTER is controlled by the FILT ENV AMT VCA. (There is no comparable attenuator for the AMP ENV GEN.) Note the P-MOD FILT switch is a redundant path for the FILT ENV GEN output. The switch is provided for OSC B to modulate the FILTER.

Details of the 3310 and associated components can be found on its Data Sheet in the Appendix.

Note that the ATK, DEC, and REL times are controlled by 0 to –5V and the SUS level is set by 0 to +5V. Accordingly, the computer inverts its normal 0 to +10V output so +10V corresponds to minimum, and 0 corresponds to maximum time. The resistor network shown for the AMP ENV GEN (R415, R407, R402...R403) divides the 10-V range by two and performs the required negative level-shift. The FILT ENV GEN is controlled in the same way.

2-8 AUDIO OUTPUT

As shown in Figure 2-4, the VOL CV follows a long path from its source on PCB 3 to the back panel, up to the control panel, and back to PCB 4. If external dynamic control such as a footpedal is used, it (instead of U372) supplies VOL CV through R113. (When troubleshooting for no audio output, check J7).

R4545 in series with U481 minimizes the possibility of oscillation with capacitive loads. R4544 reduces hum resulting when the Prophet is switched off but left connected to an energized amplifier.

2-9 MICROCOMPUTER SYSTEM DESCRIPTION

A microcomputer system consists of electronic hardware and program "software." The microprocessor (or CPU) constantly reads the program instructions from read-only memory (EPROM) which directs the processing of inputs such as switch actions, knob settings and keystrokes into switch commands and CVs for the synth. This section concentrates on hardware functions associated with this processing. The assembly-language program itself is not covered in depth as it is proprietary. But knowledge of the program is not required either to learn how the Prophet operates or to service it. In fact a good deal about what the program must do can be inferred from a thorough understanding of what the hardware does.

See Figure 2-5. If you are unfamiliar with microcomputers you might find it helpful to focus on the Data Bus, to which the CPU, Memory, and all input/output (I/O) devices connect. All processing is communicated over this bus. But since the bus can signify only a byte (comprised of eight bits) at a time, data must be transferred sequentially, a byte at a time. Conflicts between data senders and receivers—actually, bus drivers and latches—are prevented by Chip Selects (CS) generated by the Memory Address, Input Port, and Output Port Decoders. Each memory device, bus driver or latch can only send or receive data when its CS is active, and no two CSs can occur at once. Each CS is decoded from a unique combination of Address and Control Bus signals. All memory devices have A0-A9 in common. These lines signify up to 1024 (1k) addresses. Individual memory devices are differentiated by decoding A10-A12 and -MREQ into CSs which select the appropriate 1-K block. The I/O Port Decoders share A0-A5 with Memory, but only issue CSIs or CSOs when -IORQ goes low. While -MREQ and -IORQ indicate Memory or I/O can "converse" with the CPU, -WR and -RD indicate the direction of the transfer is from or to the CPU.

The Scratchpad RAM contains tables which represent the status of the switches, keyboard and knobs. In PRESET mode the Scratchpad's switch and knob tables are loaded by data from NV RAM when the current program is selected. NV RAM contains 40 such sets of programs. In PRESET pressing a switch or turning a knob is an EDIT operation which changes the Scratchpad tables, but has no effect on the original program in NV RAM unless the EDITed tables are specifically recorded (in place of the original program).

Paragraphs 2-11 and 2-12 detail how the input circuits generate data which controls the synth through the output circuits. Although it may take, for example, several thousand data bus operations to completely scan the keyboard and establish the appropriate oscillator CVs, you perceive no delay between a keystroke and the note produced because of the speed at which the program is executed. The basic program "loops" every 6 ms (166 times per second) to maintain the current status of the machine. Any status change such as a keystroke or control operation extends the loop time to about 11 ms.

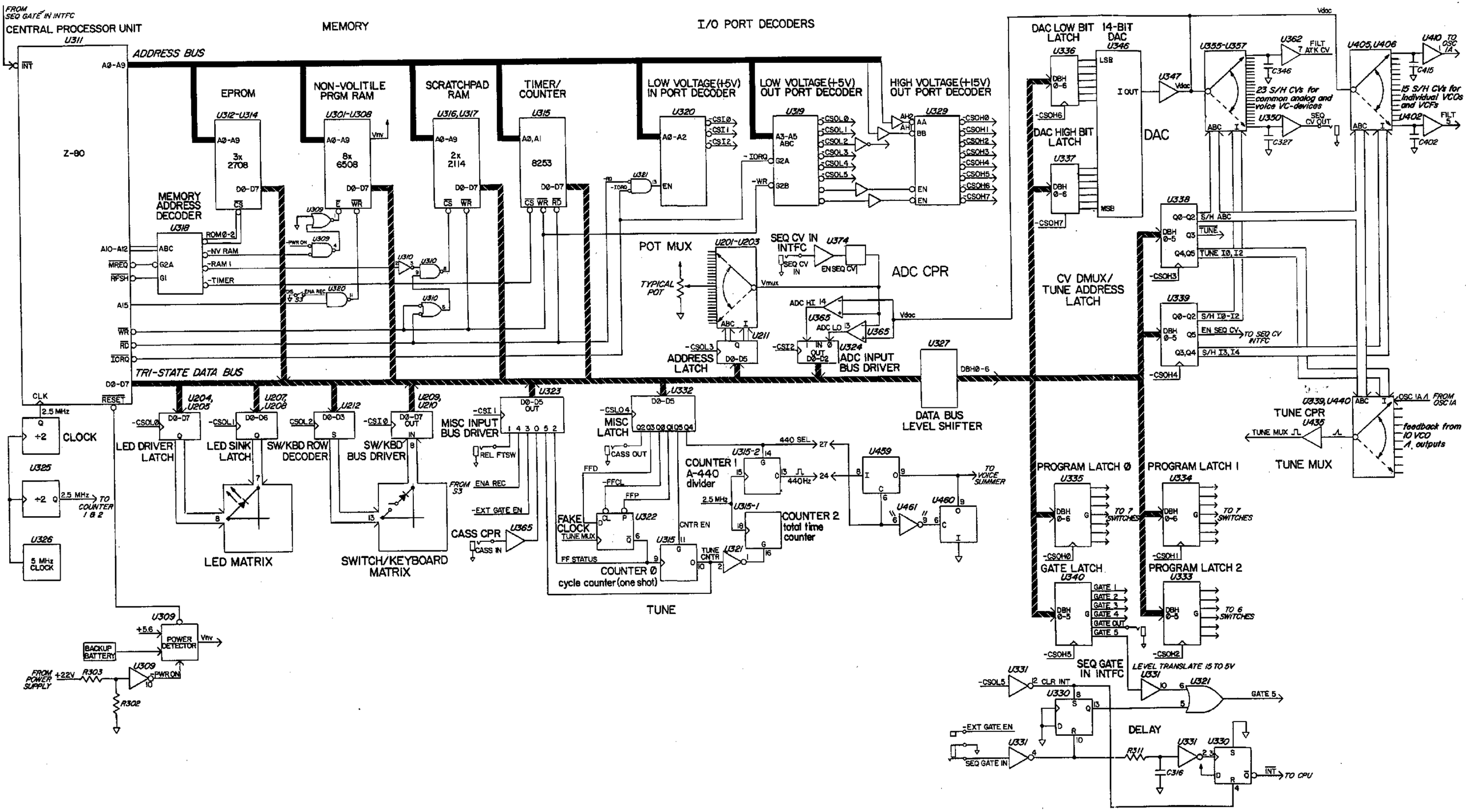


Figure 2-5
MICROCOMPUTER ABSTRACT SCHEMATIC

2-10 MICROPROCESSOR, MEMORY, AND I/O INTERFACE

Please see Figure 2-5 and schematic SD331. The Power Detector (PWR DET) circuit controls CPU start-up and shut-off through the Clock and –RESET signals. PWR DET also contains battery BT301 which provides back-up power, Vnv, for Non-Volatile (NV) RAM. The NV RAM's low current requirement allows the battery a ten-year life expectancy.

WARNING! BT301 MAY EXPLODE IF SHORTED FOR ANY LENGTH OF TIME, ALTHOUGH IT WILL USUALLY "JUST" VENT NOXIOUS GASES.

Vnv also powers U309, CMOS quad NOR gate. With power off, inverter-connected U309-10 is high. This high and that through D301 make U309-13 low holding the CPU –RESET. –RESET initializes the CPU and resets its program counter (PC) to execute the instruction in location 0000 once the Clock starts and –RESET goes high.

When power is switched on the CPU CLOCK starts immediately because the lower power supply voltages stabilize before the higher voltages. When power is switched off, the higher supply voltages decay more quickly. If the CPU is being clocked while power rises or falls, the EPROMs could conceivably cause spurious data to be written into NV RAM, since they operate on a higher voltage than the CPU (+12V as opposed to +5V). Accordingly, PWR DET immediately resets the CPU when power drops, and disables the NV RAM –CS (see below). Divider R303/R302 monitors the highest power supply voltage, which must achieve full value for U309-10 to go low. This discharges C303 through R3-1 so after about one second U309-3 goes high, starting the CPU. With the power on, D303 provides 5V for Vnv.

The Data, Address and Control Buses were basically described in the preceding paragraph. A0-A9 set up one out of 1024 addresses on all the memory chips, while the specific 1-K block CS is decoded from A10-A12, –MREQ, and –RFSH. –MREQ actually signifies the Address Bus indeed holds a valid address for a memory read or write operation. Intended for use with dynamic RAMs, –RFSH indicates the Address Bus instead holds a refresh address. Therefore to enable any memory, –MREQ must be low and –RFSH high.

A15, the most significant Address Bus line is gated with the ENABLE RECORD (ENA REC) signal through U320-11. ENA REC is pulled high by R308 unless grounded by the back-panel RECORD ENABLE/DISABLE switch which, of course, prevents unintended recording into NV RAM. Gating A15 in this way means that although NV RAM is read from memory addresses 0C00-0FFF(H), it is written into through addresses 8C00-8CFFF(H)—rather than just relying on the usual –RD and –WR signals.

–WR indicates the Data Bus holds valid data to be stored in the addressed memory or I/O device. –RD indicates the CPU wants to read data from memory or an I/O device. –IORQ indicates A0-A7 hold a valid address for an I/O operation. The –INT input is discussed in paragraph 2-15.

The Prophet's program is contained in three 2708 1024 x 8-bit ultra-violet erasable programmable read-only memories (EPROM) occupying addresses 000-03FF (ROM0), 0400-07FF (ROM1) and 0800-0BFF (ROM2). Since no write operations are performed into ROM, the appropriate CS is sufficient to place an instruction on the bus.

THE NV RAM which holds the patch programs is made from eight 6508 1024 x 1-bit CMOS static RAMs. Total current demand on the backup battery is 10 uA, or less. Many steps have been taken to protect NV, although cassette storage makes a catastrophic NV RAM failure unnecessary.

TECHNICIANS SHOULD BACK-UP PROGRAMS THROUGH THE CASSETTE INTERFACE BEFORE SERVICING. (IT TAKES ONLY TWO MINUTES.) PLAYERS SHOULD BE ENCOURAGED TO BACK-UP THEIR PROGRAMS ON CASSETTES AND/OR ON BLANK PANEL DIAGRAMS (INCLUDED IN OPERATION MANUAL), SINCE IT IS ALWAYS POSSIBLE FOR PROGRAMS TO BE LOST THROUGH THE COURSE OF SERVICE.

NV RAM read and write operations are controlled by the gated A15 and the -NV CS which is only gated through U309-4 if power is on. -NV CS causes the RAM to latch the address bus and place the addressed data on the Data Bus. The CPU acknowledges receipt of the data by setting -NV CS high. For a memory write operation, -NV WR goes low to set "WRITE MODE," and the data is written when -NV CS returns to a high state.

Two 2114 1024 × 4-bit NMOS static RAMs comprise the Scratchpad RAM. The read and write logic for SPAD is similar to that for NV, with added gating ensuring -WR or -RD is low for the SPAD RAM -CS to appear at U310-8.

U315 is an 8253 Programmable Interval Timer (PIT) used in the TUNE and A-440 circuits. For discussion, see paragraph 2-13.

As mentioned above, the I/O Port Decoders issue chip selects which control input sources and output destinations. Table 2-0 shows how all CSs are specifically decoded. Eight of the fourteen Output -CS undergo a voltage shift from 5-V to 15-V levels. The reason is that the analog switches for 10-V level waveforms in the synth must operate on +15V, therefore so must the latches which control the switches and, likewise, the decoder which controls the latches. Seven bits of the Data Bus itself are also shifted up, by U327, for compatibility with the high-voltage latches and DAC.

Table 2-0
CHIP SELECT DECODING

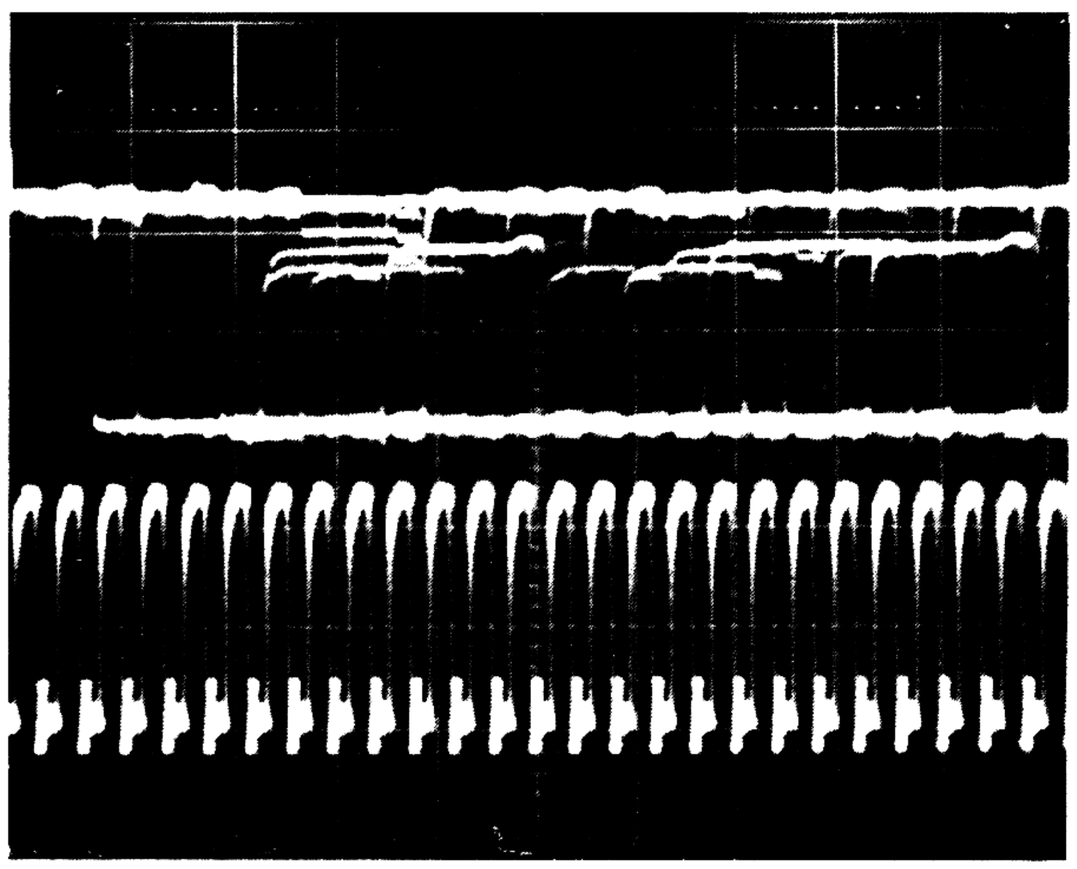
CS NAME	FUNCTION	-MREQ	-IORQ	-RD	-WR	-A10-A12	A0-A9
ROM 0	ROM 0	0	1	X	X	0	X
ROM 1	ROM 1	0	1	X	X	1	X
ROM 2	ROM 2	0	1	X	X	2	X
NV		0	1	X	X	3	X
RAM 1	SPAD	0	1	X	X	4	X
TIMER		0	1	X	X	6	X
CSI0	KBD/SW	1	0	0	1	X	01(H)
CSI1	CASS/MISC	1	0	0	1	X	02
CSI2	ADC	1	0	0	1	X	04
CSOL0	LED DRVR	1	0	1	0	X	00
CSOL1	LED SINK	1	0	1	0	X	08
CSOL2	KBD/SW DRVR	1	0	1	0	X	10
CSOL3	POT MUX ADR	1	0	1	0	X	18
CSOL4	CASS/TUNE	1	0	1	0	X	20
CSOL5	CLEAR INT	1	0	1	0	X	28
CSOH0	PROG SW 0	1	0	1	0	X	30
CSOH1	PROG SW 1	1	0	1	0	X	31
CSOH2	PROG SW 2	1	0	1	0	X	32
CSOH3	S/H ABC/TUNE	1	0	1	0	X	33
CSOH4	S/H	1	0	1	0	X	38
CSOH5	GATES	1	0	1	0	X	39
CSOH6	DAC LSB	1	0	1	0	X	3A
CSOH7	DAC MSB	1	0	1	0	X	3B

1 = DIGITAL HIGH
0 = DIGITAL LOW
(H) = HEXADECIMAL
X = DON'T CARE

For troubleshooting, it should be emphasized that most computer malfunctions are caused by failures of devices connected to the Data Bus. For example, any shorted latch input can prevent an entire data line from ever being high. Shorts between data lines will also confuse the computer terribly. Shorts may occur within a device or between the PCB traces. If you suspect a data bus problem try to pick out the line(s) with questionable levels: low should be 0-500 mV, high 4-5V (3.5V min for CMOS), as shown in Waveform 2-0A. Readings of 1V or 1.8V, for example, indicate a failure. The general procedure is to first remove socketed PCB 3 devices: CPU, EPROM, SPAD RAM, and NV RAM—WHICH WILL CLEAR THE PROGRAM MEMORY! If this doesn't locate the problem you may have to cut traces. REMEMBER—SINCE THE COMPUTER WAS OBVIOUSLY RUNNING AT ONE TIME, THE SHORT IS MORE LIKELY TO BE DEVICE FAILURE THAN A PC-SHORT, SO BE SURE TO CHECK ALL POSSIBLY BAD COMPONENTS BEFORE CUTTING TRACES. The customary technique is to make the first cut at the electrical center of a bus line to isolate the problem to one half or the other. Then halve the trace again, and so on, until correct levels are restored. To prevent other malfunctions, cut traces should usually be repaired just after they have yielded information on the direction of the short. Note that a short on the high-voltage data bus (DBH) will not usually degrade computer operations since DBH is buffered from DB. However it will be easy to check DBH for malfunctioning switch bits, GATE bits, or S/H addresses.

A DBO, U311-14

B 2.5 MHz CLOCK



V: 2V/div
H: 1 us/div

Waveform 2-0
DATA BUS AND CLOCK

2-11 CONTROL MATRICES

This paragraph describes how the computer scans the control panel to learn what keys or switches have been pressed, and to light the LEDs imbedded in switches that are on. As input devices, switches and keys are scanned indentically. In both cases the microcomputer maintains tables in Scratchpad RAM which correspond to the status of the Switch/Keyboard Matrix (SW/KBD MTX). That is, each switch or key has a corresponding memory bit which is set (1) or reset (0) if the switch or key is on or off. Although similar in structure the switch and keyboard tables are interpreted quite differently. For example the W-MOD FREQ A switch bit causes a digital output to close or open a solid-state switch, and light or extinguish its LED. But a key bit is converted to a key number (1 - 61) which becomes an OSC FREQ CV through the DAC. In addition, the fact of a key going on or off must be stored for voice assignment and generation of the GATEs.

The SW and LED MTX are divided across PCBs 1 and 2; principal components being shown on schematic SD232. The keyboard is wired into the SW MTX through J201. The LED MTX includes all the elements of DS224 dual BANK-PROGRAM display; all seven-segment decoding being done by software.

The program scans the keyboard first. The basic procedure is to activate one matrix row of eight consecutive keys, then check the intercepting columns for the presence of a bit. The resulting data sent to the CPU by the column bus drivers uniquely identifies a combination of switch closures in each row.

Specifically, to scan the first eight keys the CPU sends the number 08(H) to the SW/KBD ROW DECODER by clocking -CSOL2. This selects S8 (U212-18), which holds the first matrix row high. If C0, E0, and G0 happen to be held, the number 10010001 (91H) will be sent to the CPU when it clocks the bus drivers with -CSI0. This number is then placed in Scratchpad; becoming the first byte in the keyboard table. To read the next key row the CPU increments the driver to set S9, and reads the second key table byte.

Switches are scanned to fill a Scratchpad RAM table in the same way when the CPU sets the driver S0-S4. The diodes wired throughout the SW/KBD MATRIX allow n-key rollover, which is the simultaneous pressing of any number of switches and keys. They prevent switched bits from returning through other closed switches on the same column, which would activate other rows.

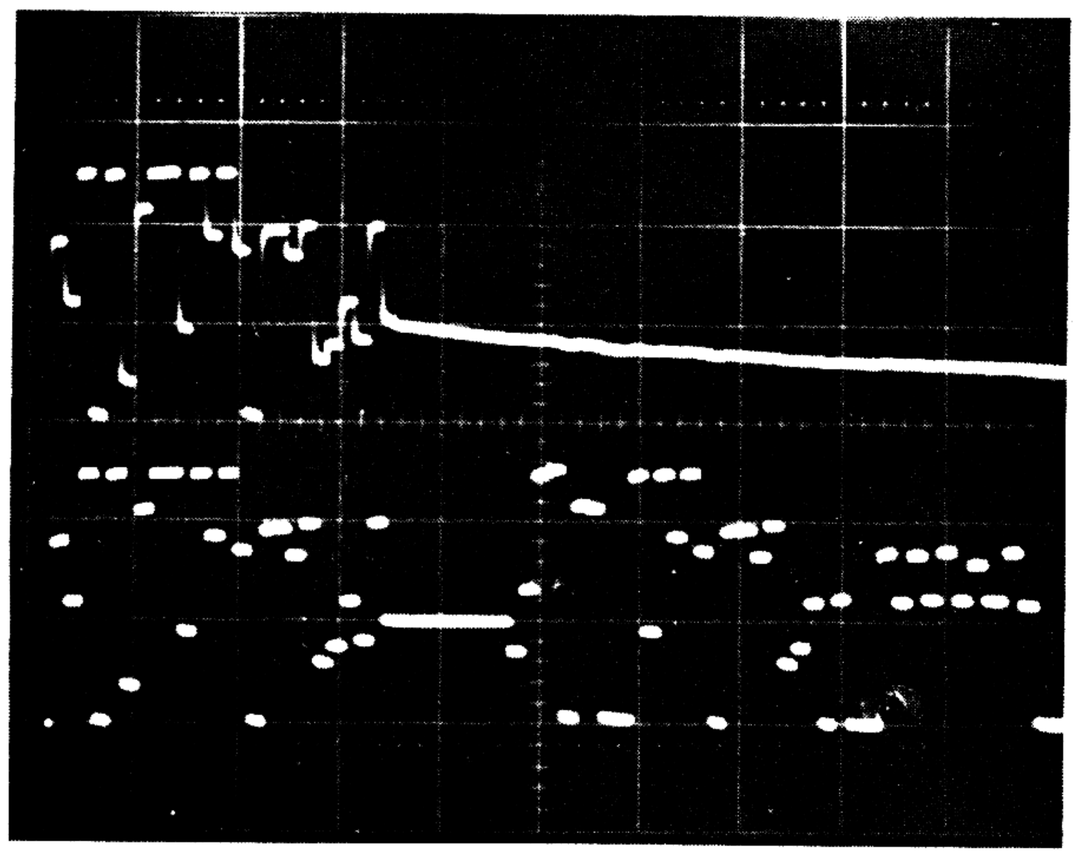
For troubleshooting it must be emphasized that most keyboard problems are caused by dirty, bent, or broken J-wires. Dead notes not caused by J-wires usually occur in groups of eight, making it easy to isolate the problem row or column. If a switch does not function and its LED doesn't light, the problem must be in the SW MTX. Check other switches to isolate malfunctions to a single row or column. If the LED lights but the function is not enabled, the problem must be in the corresponding output latch, solid-state switch (4016), or analog circuitry.

The LED matrix operates on the same line-by-line technique used to scan the switches and keys. In fact, the LEDs are "mapped" similarly to the switches so the two tables will correspond. First a number from the Scratchpad LED table representing active LEDs in the first column is latched by the LED DRIVERS U204/5 as port -CSOL0. Then the first column is pulled low—causing current to flow through LEDs whose anodes are being pulled high—through U206-10 by latching data 01(H) to U207/08 LED SINK; port -CSOL1. To output the next column, the CPU sends the next LED table byte to the LED DRIVERS and rotates the LED SINK bit to pull the second-row cathodes low, and so on. The LEDs are therefore not constantly lit, they only seem so due to persistence effects accompanying our sight. Some owners may notice a slight difference in brightness between the BANK and PROGRAM numeric displays, or complain of them flickering while playing. Both effects are normal, resulting from different scan times for each display, and from the lengthening of the "loop" time with each new keystroke.

2-12 ADC, DAC, AND CV OUTPUTS

The DAC is the essential interface between the control potentiometers and microcomputer and between the microcomputer and the synthesizer. It is based on the 16-bit, integrated DAC-71-CSB-I. However, at most, 14 bits are used only for precisely controlling the oscillators while, normally, seven bits provide adequate resolution for all other computer-processed CVs. The DAC's full scale voltage is 10.67V, but most CVs are limited to 10V by the software.

For editing or manual operation, the DAC performs analog-to-digital conversion (ADC). This is done by outputting one of 24 entries from a Scratchpad RAM table of pot settings, at the same time the actual pot is being sampled through the ADC "window" comparator (ADC CPR). (Actually, the 10-V DAC range is divided by two for comparison with 5V-range pots.) The comparator signals ADC HI or ADC LO if the pot wiper is actually set below or above the value of the converted table entry. As long as the voltages don't match, the table value is decremented or incremented until they do match. Once all the pots have been checked, a few adjustments are made (depending on the mode of operation), and the DAC again converts the pot values, this time distributing them and the oscillator and filter CVs to the synth. Thus, the DAC output, Vdac, steps between 62 values (24 pots + 38 CVs) (during each 6-ms loop. The POT MUX output, Vmux, assumes the value of the settings of all 24 pots during the first part of each loop. This is shown in Waveform 2-1a. In Waveform 2-1b, Vdac is shown assuming the 24 comparative pot values and the 38 CVs.



A VMUX, U365-9

B VDAC, U364-7

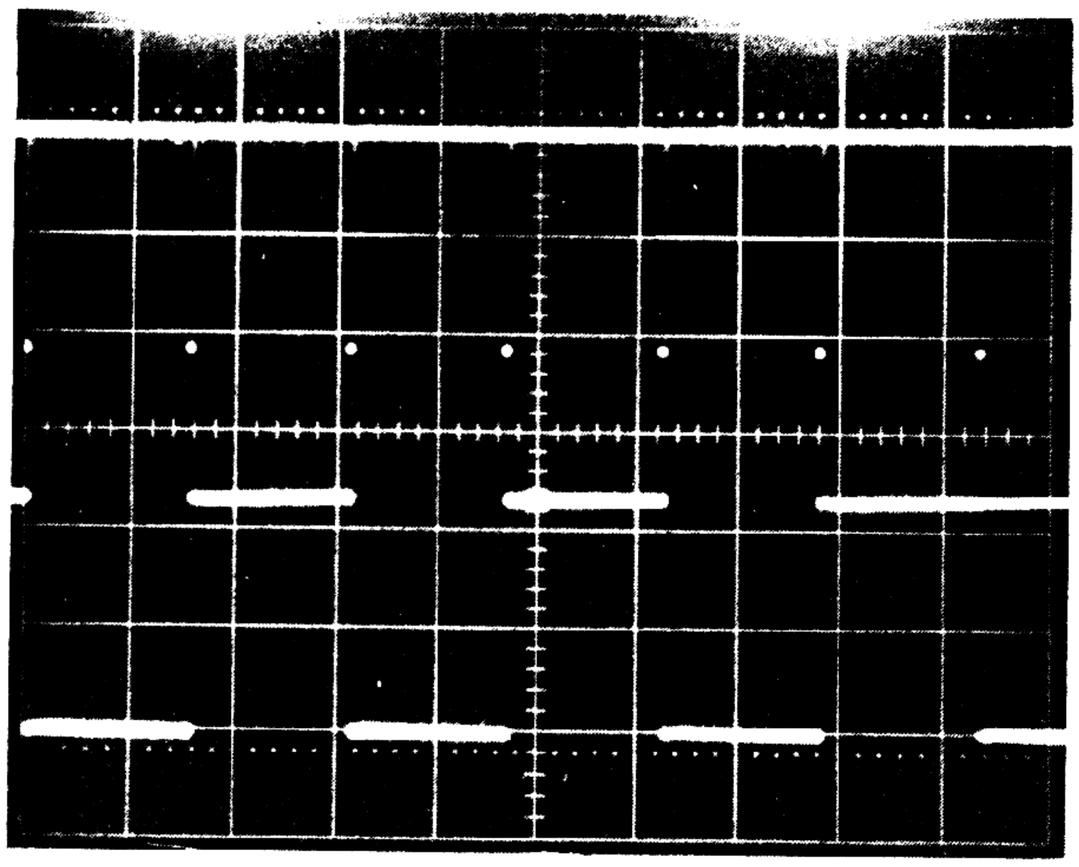
V: 2V/div
H: .5 ms/div (approx.)

Waveform 2-1
VMUX AND VDAC

The POT MUX is shown on SD231. Basically, data latched by U211 selects (or, addresses) one of 24 pots at a time, whose wiper voltage becomes the Vmux sent to the ADC comparator. The address latch bits Q0, Q1, Q5 have a decimal value 0-7. Waveform 2-2 shows Q0 toggling when clocked. Applied to the A, B, C, inputs of U201-03, these bits simultaneously select one of eight inputs on each 4051. When high the I inputs inhibit the 4051; so to select just one pot, Q2, Q3, or Q4 must be low.

A –CSOL3, U211-9

B Q0, U211-2



V: 2V/div
H: 50 us/div

Waveform 2-2
POT MUX LATCH

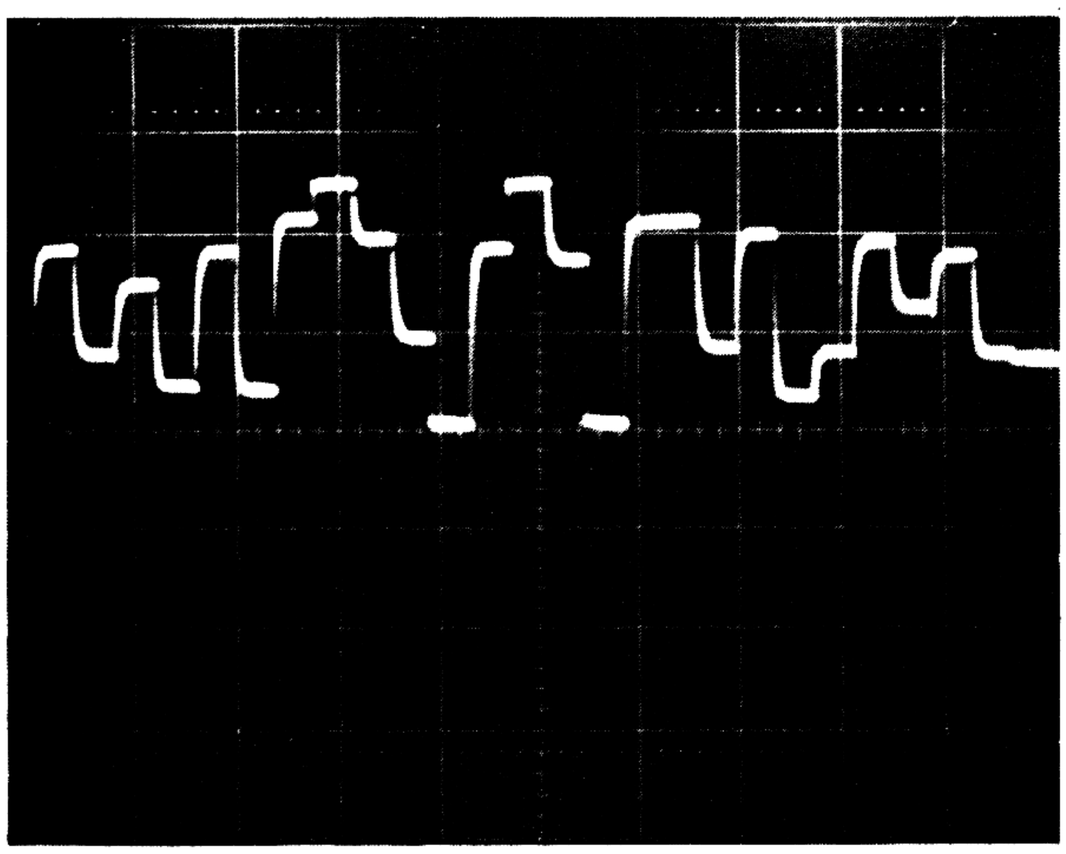
U211's state is undetermined on power-up, since the computer has not yet had time to initialize the POT MUX by setting all inhibits high. U211 might well "come up" with more than one low for Q2, Q3, and Q4. In such cases two or more pots would be connected together at Vmux. The current surge resulting from any significant potential difference between their settings would instantly destroy a 4051, were it not for R203/R206/R209.

To check the pots the CPU first places data 18H on the bus and clocks the POT MUX address latch with –CSOL3. This sets Q2 and Q4, inhibiting U201 and U202. With Q3 reset (0), U203 connects R105 FILT ATK wiper from pin 13 to 3. If the knob is set halfway, +2.5V (Vmux) will appear at the common input of the ADC CPR, U365-9/10 (see schematic SD332).

Next the CPU takes the first pot table byte from SPAD RAM, places it on the bus, and latches it to the DAC HI latch U337 (and U342-5), port –CSOH7. If we assume this pot has not changed position since the last loop, the converted data should compare with Vmux. Thus data 3C(H) pulls DAC bits 11, 12, 13, and 14 low through U344/45 inverters. The DAC has a current output which U347 converts to voltage, in this case 5V (2.667 + 1.333 + 0.666 + 0.333V). R334/35 and R336 divide by two so 2.5V appears at U364-7. Since this equals Vmux, neither comparator output goes high. The network containing D306/07, and R366-71 provide "hysterisis", such that the difference between Vdac/2 and Vmux must be more than 34 mV before the comparator will activate. Pot drift is also eliminated through software hysterisis which watches the direction of pot changes. A pot must move two steps in the same direction to qualify as a legitimate change. To check the remaining pots, the CPU latches data 19-1F, 28-2F, and 30-37(H) to port –CSOL3. When done, data 38(H) clears the POT MUX. Waveform 2-3 details Vmux.

Having updated its Scratchpad RAM tables of switch and key status and of pot values, the CPU is now ready to output the appropriate CVs. Certain adjustments need to be performed, such as figuring the tuning biases according to the notes to be sounded (see paragraph 2-13), and inverting the envelope generator timing voltages (see paragraph 2-7). If UNISON mode is on, the KBD CVs are removed from the OSC S/Hs. GLIDE CV is also switched on in UNISON.

VMUX, U201-3



2V/div
.2 ms/div

Waveform 2-3
VMUX

The CV DMUX is the reciprocal of the POT MUX. In fact it uses the same 4051 devices, though wired so a single input can be routed to one of 38 destinations. As in the POT MUX, CV destinations are addressed by data latched from an output port. And since CV distribution is sequential, a short-term sample/hold (S/H) analog memory is provided at each destination to ensure the synth is isolated from the pulsing Vdac. Each S/H consists of a low-leakage capacitor in shunt with the non-inverting input of a TL082 JFET-input op amp (BIFET) voltage follower. The BIFET has extremely high input impedance—several thousand megohms. The computer-output process of strobing the S/Hs only allows a few microseconds for each S/H to acquire a specific value of Vdac. The S/H capacitor is large enough to hold this charge for 11 ms (the longest loop time) but low enough to quickly recharge to a higher or lower Vdac when next strobed. Between strobes, or whenever the 4051 is inhibited, the S/H output remains constant because there is no discharge path for the capacitor. As a practical matter S/H output can be expected to "droop" up to 1/2-mV over 7 ms. Droop greater than this is usually BIFET failure (input leakage). Of course capacitors can also leak, and if open, will make the S/H output pulse.

Using the FILT ATK example above, data 3C(H) is again sent to the DAC through port -CSOH7, producing a Vdac of 5V (Remember that the six ENV GEN timing CVs are inverted in software). Port -CSOH4 S/H STROBE latch U339 (see schematic SD333) sets S/H I0, I1, I2, I3, and I4 all high, inhibiting all DMUX 4051s. Port -CSOH 3 latches data 00. S/H I0 then goes low enabling U357 which strobes C346 and U362-7 with 5V. I0 returns to a high state, completing the first strobe. In short, the DMUX 4051s are always inhibited while Vdac is changing value.

To set oscillator pitch, first the most significant DAC bits are latched through -CSOH7, then the least significant DAC bits are latched through -CSOH6. The Individual CV DMUX is located on PCB 4, controlled by S/H A, B, C, I3, and I4 (see schematic SD430).

2-13 TUNE AND A-440

The synthesizer and microcomputer circuits employed for polyphony and programmability having been covered, this paragraph explains the third main feature resulting from the Prophet's A/D hybrid technology. The TUNE system has only been briefly mentioned before, but it is responsible for the entire performance of the instrument in the sense that without its corrective influence, the Prophet's ten voice oscillators could not be expected to stay in tune over their nine-octave range. The reasons for this are several.

There are two basic parameters to work with in tuning. One is initial frequency (INIT FREQ) that is, the specification that all ten oscillators sound the same pitch given the same, steady CV. The other is SCALE (or, V/OCT), which desires a predictable pitch change to accompany a specified CV change. INIT FREQ errors can be introduced by any of the many sources of oscillator control. While summing resistors in the Common Analog circuitry are precision-matched, errors may still result from the combination of MTUN, P-BND, W-MOD, UNISON, and FINE (on OSC B). In the voices the A SUM and OSC S/H CV summing resistors and P-MOD FREQ A circuits are error sources. SCALE errors generally occur in the VCO itself. For example, while a CV change from 1V to 2V may produce an exact octave interval, a change of 5V to 6V might cause a pitch change of greater or less than an octave. All VCOs have this error to some degree somewhere in their range. For an IC, its associated components, such as the SCALE trimmer, can contribute error. Chips age, and their parameters will change with changing temperature—although this effect is significantly reduced with on-chip temperature compensation circuitry (see Appendix).

Actually, TUNE has two stages, only the first of which occurs when the TUNE switch is pressed. In less than ten seconds the microcomputer samples each VCO frequency at octaves, while using successive-approximation to determine the exact 14-bit CV required to tune the VCO to a reference. The system measures the period of each oscillation in terms of CPU clock cycles. The difference between the ideal, 83mV-step CV which should produce the reference frequency and the 14-bit, 651-uV CV which actually does so is called bias. Biases for each oscillator are determined at the ten C's (C0 - C9) across the VCOs' full range. The biases are placed in a 200-byte table in Scratchpad RAM (1 bias/oct × 10 oct × 2 bytes/bias). The second stage of TUNE occurs while playing. Whenever an OSC S/H CV is to change in response to a keystroke, the computer determines the new note's position between octave bias-points, and calculates the exact bias for that semitone.

U433/40

The first stage functions as follows. First the CPU disables the PITCH wheel, MTUN, and UNI CV, by opening switches in their signal paths. The TUNE circuit consists of ~~U339/40~~ TUNE MUX (see Figure 2-5 or schematic SD430), U435 TUNE CPR, and Counter (CNTR) 0 and 2 of U315, a three-section 8253 Programmable Interval Timer. (CNTR 1 is used for A-440, discussed below). When activated, the TUNE MUX sequentially connects each oscillator output to the TUNE CPR in the same way the POT MUX samples pots for the ADC CPR. The TUNE CPR converts the sawtooth to pulses. With no input at U435-3, R4158/R4159 hold U435-2 at 1.36V, so U435-7 is high. U435-3 increases with the positive-going sawtooth, so that when it crosses 1.36V, U435-7 goes low. R4170 feeds-back the transition to prevent oscillation (hysterisis).

The TUNE flip-flop (FF) must be explained in conjunction with the 8253. The PIT contains three independent, multi-mode, 16-bit presettable down-counters addressed as memory locations 1800-1802(H), plus a control word register at 1803(H). TIMER -CS must be low for all write or read operations. -WR or -RD indicate the CPU is writing a control word or count, or expecting a count. During initialization (on power-up) each counter's mode is programmed by a byte written into the control word register. CNTR 0 operates in "one-shot" mode. It is programmed to, at first, count one oscillator pulse. But the 8253 actually requires an extra clock pulse—which we call a "fake clock"—to accurately begin the count. Therefore each oscillator sampling is preceded by the fake clock pulse from the TUNE FF, under control of U332, port -CSLO4 (see schematic SD332). After the fake clock pulse, FFD goes high, allowing the TUNE FF to invert TUN MUX through -Q (U322-6).The TUNE FF is then constantly cleared in preparation for each new oscillator pulse.

With CNTR 0 enabled by CNTR EN at U332-5, OUT0 (U315-10) goes low at the first oscillator edge from the TUNE CPR. U321-1 inverts this to a high which gates CNTR 2. CNTR 2 is programmed to count CPU clock cycles, so it decrements at the rate of 2.5 MHz. When CNTR 0 reaches its terminal count, that is, when one pulse (in addition to the fake clock) has been counted, OUT0 goes high, stopping CNTR 2. CNTR 2's 16-bit register now represents the number of CPU clock cycles occuring during one period of OSC 1A's sawtooth. This number is compared to a reference. An oscillator that is too sharp will have a lower count than the reference, and vice versa. As long as the count and reference don't match, the CPU adjusts the OSC S/H CV and samples the sawtooth again. Successive approximation starts with the DAC MSB, setting each bit which does not cause the oscillator pitch to overshoot the reference.

After tuning OSC 1A at C3, the reference count is halved to tune C4, since one cycle at C4 should take exactly half the number of CPU clock cycles than at C3. For octaves C5 - C9, the cycle count in CNTR 0 is doubled instead (2, 4, 8...32). The C0 - C2 biases are actually extrapolated from the curve suggested by the C3 - C9 bias table, rather than found by direct measurement because counting such low-frequency pulses would take an inconvenient amount of time. The remaining oscillators are tuned in the same way.

When enabled by U332-12, CNTR 1 simply divides 2.5 MHz by 5682 to produce the 440-Hz square wave summed into the AUD OUT stage (see SD430). To prevent noise, the A-440 input is grounded by U460-9 when not in use, by inverter-connected U461-9.

2-14 SEQUENCER INTERFACE

The sequencer interface is intended for use with SCI's Model 800 Digital Sequencer, although the design is flexible enough to interface with many types and qualities of analog inputs. For sequence recording the Prophet outputs the keyboard CV and a trigger pulse for the most recently played note in polyphonic mode, and for the lowest note played in UNISON mode. To playback, the sequencer sends the same CV and trigger pattern to the Prophet, which digitizes the SEQ CV IN for control of Voice 5.

The Prophet's sequencer output (record) circuitry is the same as the synthesizer output circuitry. SEQ CV OUT appears at S/H U350-7 before buffering by voltage follower U348-6 (see schematic SD333). The SEQ TRIG OUT is a bit latched by port -CSOH5, U340-2.

The sequencer input (playback) circuitry is a bit more complex (see schematic SD332). Connecting SEQUENCER.GATE IN closes a switch on J3 grounding U323-10. When port CSI1 is input, this low notifies the computer to process the two SEQ inputs. SEQ CV IN is assumed to be an analog voltage which slews between its various values. The slew rate will vary with the type of sequencer (or other accessory). Ideally, the input device only produces its GATE once its CV output has fully stabilized. However, in the worst case some accessories will continue to slew after producing the GATE. For this reason the Prophet delays the SEQ GATE IN to allow SEQ CV IN time to settle, by using the interrupt (-INT) feature of the CPU.

During initialization the Z-80's interrupt mode is programmed so that a low on the -INT pin forces the program to restart at memory location 38(H) (when the interrupt has been software-enabled). This is the starting address of the SEQ HANDLER subroutine. Initialization also clears the -INT through port -CSOL5. U331-12 inverts this -CS to +CLR INT which resets U330-4, making -Q high. U330-13, Q remains low, being held reset by U331-4. When a GATE appears, U331-4 goes low and U331-2 goes high after a 2-ms delay through R311/C316. This high clocks U330-3, producing the -INT pulse at U330-2.

When it receives the -INT, the CPU completes its current instruction, placing the next instruction address and register statuses on the "stack", then enables the SEQ CV IN by latching EN SEQ through port -CSOH4, U339-2 (see schematic SD333). This bit closes switch U371-9, connecting the SEQ CV IN to the ADC CPR. The SEQ CV is then determined through successive-approximation and stored in a Scratchpad table for later addition to Voice 5. After the voltage is processed, the CPU again clears the interrupt. However, this time U330-13 goes high, gating voice 5, because U330-10 is being held low by the SEQ GATE IN through U331-4. When SEQ GATE IN turns off, U330-13 is again reset.

2-15 CASSETTE INTERFACE

The cassette interface hardware is simple (see schematic SD332). For storing on tape, bits are serially-latched out through MISC output port -CSOL4, U332-7, filtered by R324/C351, and ac-coupled to the recorder input by C352. For loading from tape, the pulses are ac-coupled by C361 and squared-up by the CASS CPR which, as a zero-crossing detector, is insensitive to phase or polarity variations between recorders. R343 and R344 form a divider parallel with divider R342, R430, R337, and R341, each having a threshold of about 0.9V. D305 clamps the pulses to not exceed -0.6V. Read bits are input through MISC input port -CSI1. Since allowance must also be made for speed variation, a technique of counting edges rather than identifying logic states must be used.

Organized as 40 24-byte programs, NV RAM contains 960 bytes. The least-significant seven bits of each byte represents a pot setting of 0 - 127 steps, while the MSB represents a switch setting (1=on, 0=off). (When selecting a program in PRESET mode, a set of twenty-four bytes is transferred to the Scratchpad, with the pot bits filling the pot table and the switch bits being regrouped into the switch status table.) Interface timing is based on a unit called a minim, which is equivalent ot 232.4 us. Each bit is transmitted or received over a 12-minim period (2.8 ms), with a few microsecond space between them. To write, the interface simulates frequency-shift keying (FSK) by toggling the output latch every minim to indicate a 1, and every fourth minim to indicate a 0. These rates correspond to approximately 2151 Hz (1/234 us × 1/2) and 538 Hz (2151 Hz/4). When reading from tape the interface counts the edges received and loads a 1 or 0 into NV RAM depending on whether the number of edges is greater or less than seven. The absolute number of edges need not be detected in any specific period, thus providing range to accommodate wow and flutter in the cassette deck.

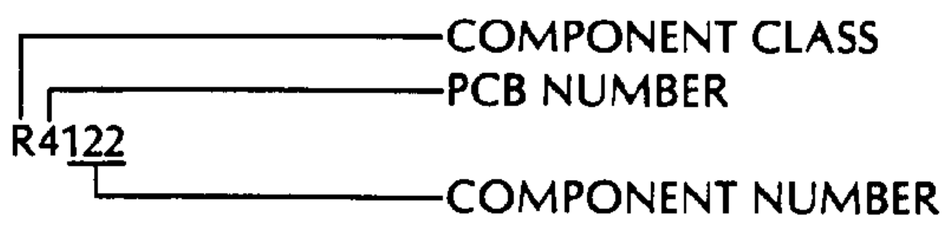
SECTION 3
DOCUMENTS

3-0 DOCUMENT LIST

3-1 DOCUMENT NOTES

These notes explain component designation and the use of symbols on our documentation. For glossary of abbreviations, see Section 6.

Component designators include three items of information:



COMPONENT CLASS is symbolized by standard letters, for example, U for integrated circuit, RT for temperature-sensitive resistor, and DS for indicator.

PCB NUMBERS are:

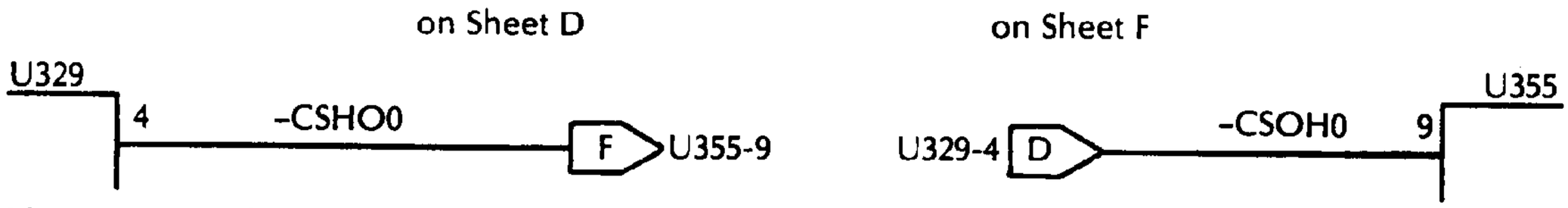
PCB 1 RIGHT CONTROL PANEL
PCB 2 LEFT CONTROL PANEL
PCB 3 COMPUTER BOARD
PCB 4 VOICE BOARD
PCB 5 POWER SUPPLY BOARD

No PCB NUMBER is given for chassis-mounted components.

COMPONENT NUMBERS are sequenced according to their position on the PCB.

We bus lines together to prevent long, confusing parallel runs. For example, DATA BUS lines are drawn as a single line, with individual lines symbolized DB0, DB1, DB2...where the bus "fans-in" or "fans-out" at a device. If there are no DB (or A, ADDRESS BUS) symbols, the bus lines are assumed to connect according to the device pin names.

Although bussing wires reduces the number of interrupted signals, some breaking of lines on a page or continuation of signals between pages cannot be avoided. At these points you will find symbols such as:



The pointers indicate signal flow. The sheet letter symbol is found in its margin.

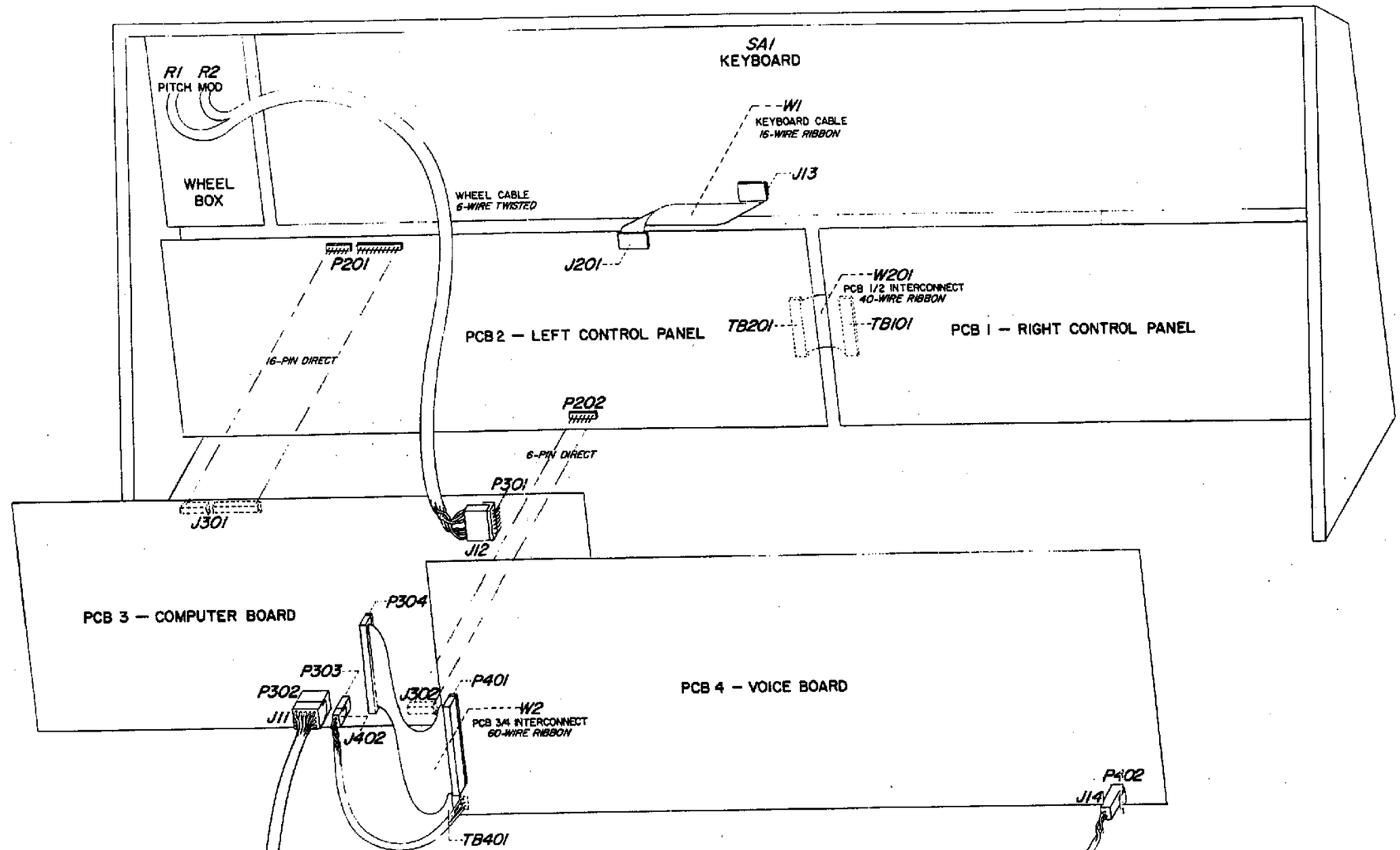
Connectors are drawn according to whether the pins are male or female, so the arrows do not necessarily indicate signal flow.

Zeros are slashed (Ø) only where needed to prevent ambiguity.

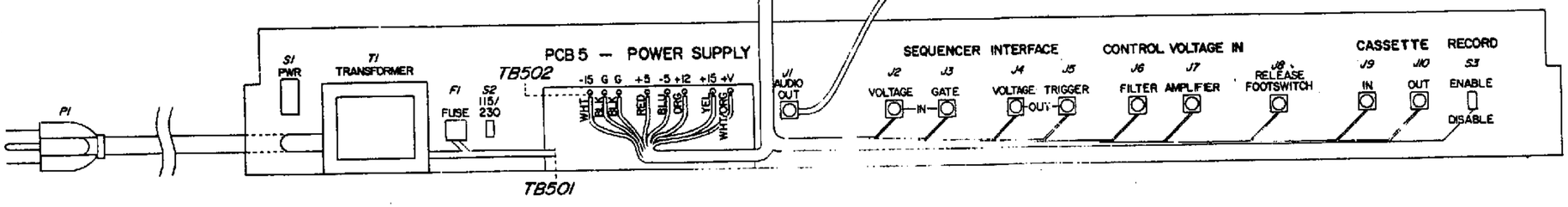
Power and ground connections for multi-device packages have been shown on the first device in the package, except where the first device is not presently used.

Unless otherwise indicated resistances are in ohms and capacitances are in microfarads.

TOP PANEL ASSEMBLY



BOTTOM PANEL ASSEMBLY



CHASSIS

LAST	NOT USED
F1	
J14	
P1	
R2	
S3	
SA1	
T1	
W2	

SEQUENTIAL CIRCUITS INC

TITLE: INTERCONNECTION

SIZE: D — 1000.3

DWN: 3/1/79

APP:

DOCUMENT No. BD031

SHEET 1 OF 1

LTR	REVISION	DATE	DWN
105		3/12/79	

SEQUENTIAL CIRCUITS INC	
TITLE	PCB1 PARTS ID
DSN	SIZE D · MODEL No. 1000.3
DWN	7/17/80 · DOCUMENT No. PP 131
APP	
ISS	SHEET 1 OF 1

	DATE		REVISION

TB101/201

28 36 21 — SD1 SD3 SD4

31 32 22 30 20 19 25 23 — SR0 SR1 SR2 SR3 SR4 SR5 SR6 SR7

3 2 1 17 18 13 14 15 11 5 6 — +5a

37 LR4

DSI04 FROM CASSETTE

DSI03 TO CASSETTE

DSI14 TUNE

DSI02 A-440

35 LD0 — DSI05 PS1

39 LD1 — DSI06 PS2

27 LD2 — DSI07 PS3

29 LD3 — DSI08 PS4

26 LD4 — DSI09 PS5

24 LD5 — DSI10 PS6

38 LD6 — DSI11 PS7

33 LD7 — DSI12 PS8

DSI13 RELEASE

DSI01 FILT KBD

34 LR1

40 LR3

PROGRAM SELECTS

SI04	DI04	FROM CASSETTE
SI03	DI03	TO CASSETTE
SI14	DI14	TUNE
SI02	DI02	A-440
SI05	DI05	1
SI06	DI06	2
SI07	DI07	3
SI08	DI08	4
SI09	DI09	5
SI10	DI10	6
SI11	DI11	7
SI12	DI12	8
SI13	DI13	RELEASE
SI01	DI01	FILT KBD

RI01	FILT CUTOFF (10K, LIN)
RI02	FILT RESONANCE
RI03	FILT ENV AMOUNT
RI05	FILT ATTACK
RI06	FILT DECAY
RI07	FILT SUSTAIN
RI08	FILT RELEASE
RI09	AMP ATTACK
RI10	AMP DECAY
RI11	AMP SUSTAIN
RI12	AMP RELEASE

12 16 4 8 — +5a — CI01 .1

9 VOL CV IN

10 VOL CV OUT — RI13 10K, LIN — VOLUME

+5a — RI04 — 7 MTUN — MASTER TUNE

1. ALL POTS 10K, LIN
2. SI01/13 ARE BLACK
   SI02-12 ARE GREY

LAST	NOT USED
CI01	
DI14	
DSI14	
RI13	
SI14	
TBI01	

3-5/3-6

SEQUENTIAL CIRCUITS INC

TITLE: PCB1 CONTROLS

DSN

DWN

APP

SIZE D — MODEL NO. 1000.3

DOCUMENT NO. SD131

SHEET 1 OF 1

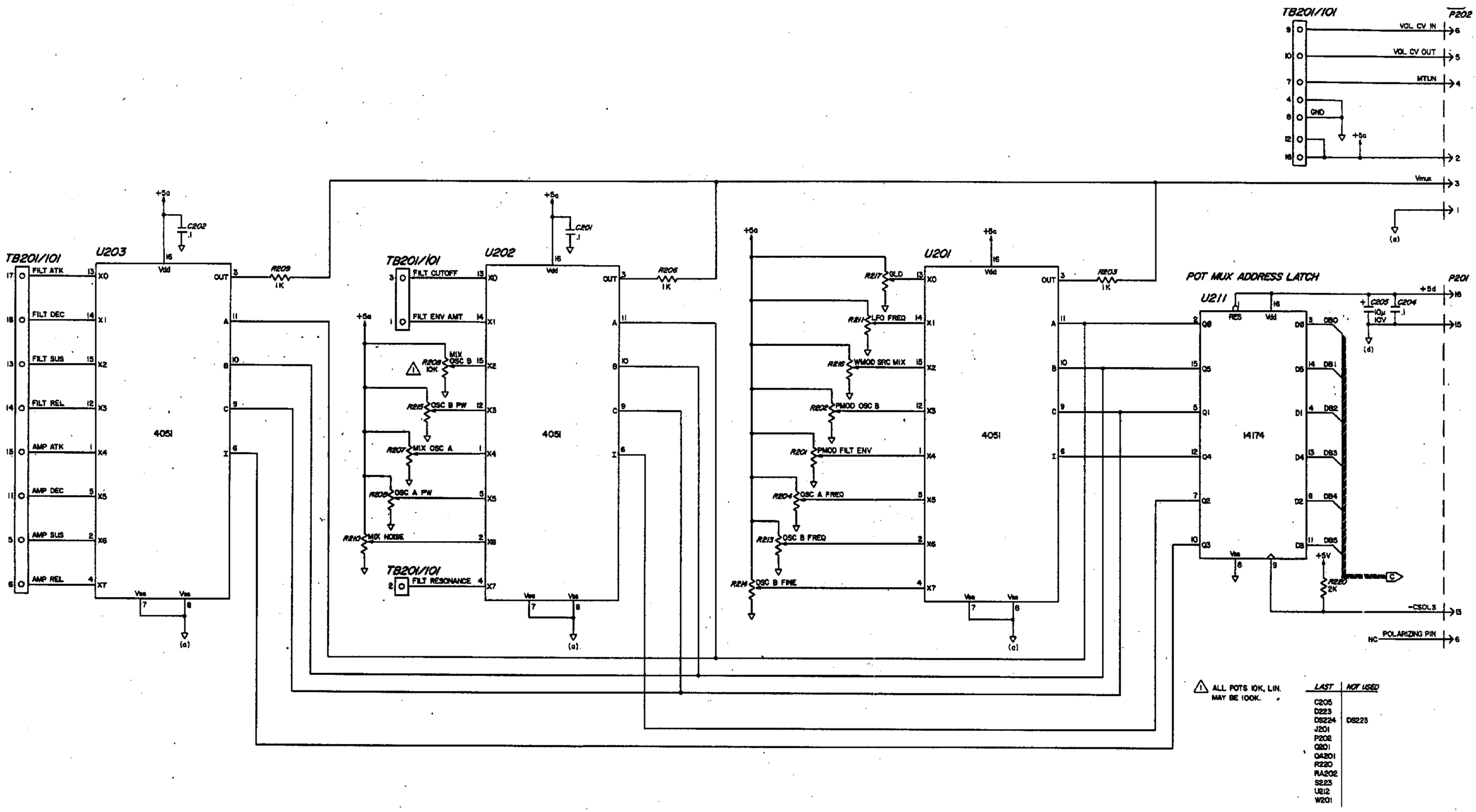
REVISION | DATE | APP'D

SEQUENTIAL CIRCUITS INC

TITLE: PCB 2 PARTS ID

DSN	DATE	SIZE E	MODEL No. 1000.3
DWN [signature]	7/17/80	DOCUMENT No. PP 231	
APP			
ISS [signature]	9/17/80		SHEET 1 OF 1

PART LAST S/N	DATE	ECN No.	REVISION	LTR



⚠ ALL POTS 10K, LIN. MAY BE 100K.

LAST	NOT USED
C205	
D223	
DS224	DS223
J201	
P202	
Q201	
QA201	
R220	
RA202	
S223	
U212	
W201	

SEQUENTIAL CIRCUITS INC

TITLE: PCB 2 POT MUX

DWN

CHKD

APP

MFG

SIZE D | DWG. No. 1000.3 | DOCUMENT No. SD231 | SHEET 1 OF 2

DATE | REVISION

U204 +5d QA201 3082 RA201 LED MATRIX TB201 TO PCB 1 U212 +5d SWITCH/KBD MATRIX

U205 LED DRIVER LATCH

P201 -CSOL0 -CSOL1 -CSOL2 -CSI0

U206 U207 U208 2003 4042

LED SINK LATCH

4514

SW/KBD ROW DECODER

W1 KEYBOARD CABLE NOT SHOWN

SW/KBD STATUS BUS DRIVER

½RA202 ½U209 ½U210 4503

SAI KEYBOARD

SPARES:

½RA202 RESISTOR PACK ALL 22K

½U209 ½U210 4503

⚠1 S201-21 ARE BLACK S222/24 ARE GREY S223 IS ORANGE

⚠2 CONTROLS IN PARENTHESIS ARE ON PCB1

SEQUENTIAL CIRCUITS INC

PCB 2 CONTROL MATRICES

DRN

DWN

APP

SIZE D

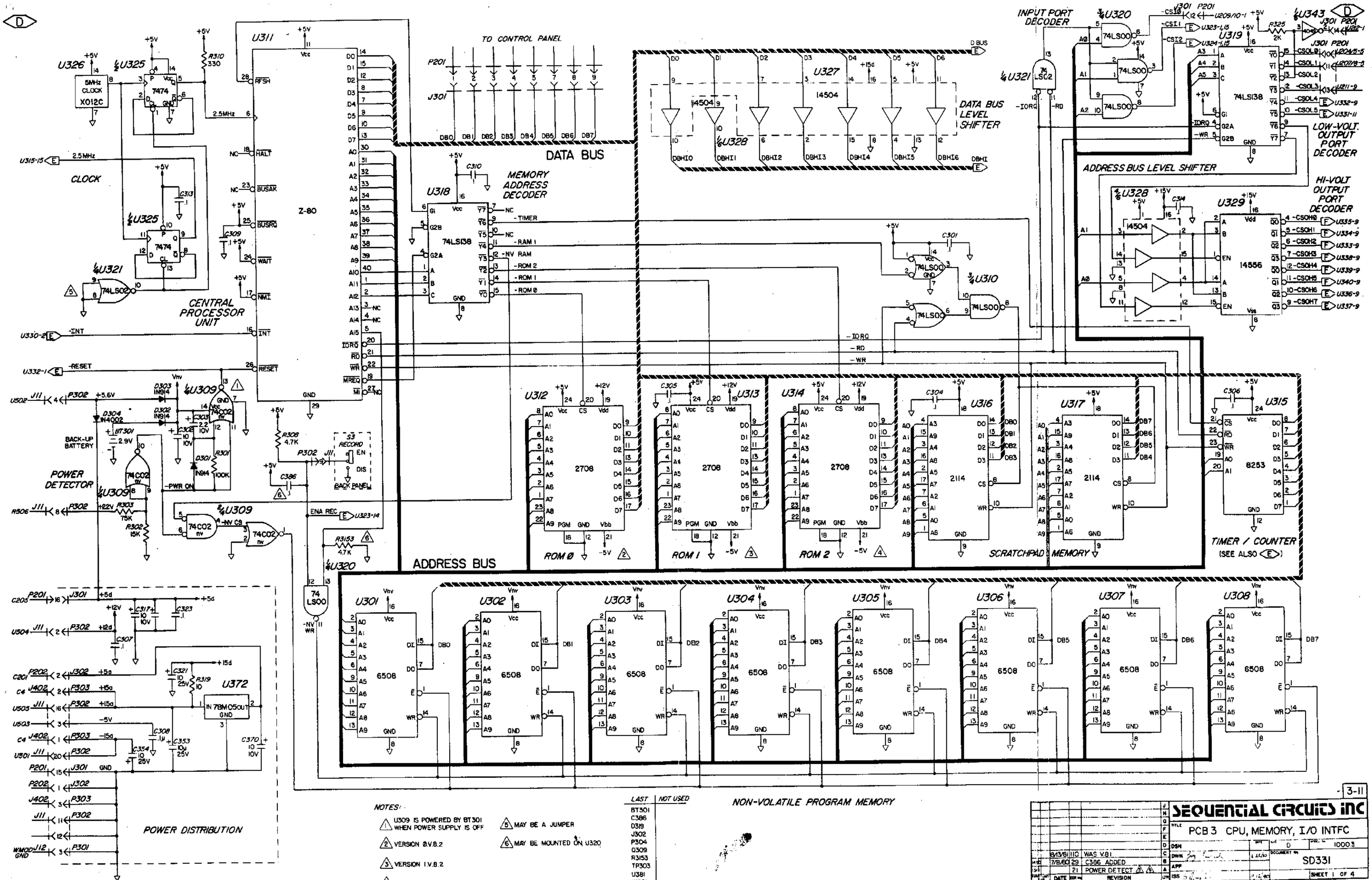
DRAWING NO. SD232

SHEET 2 OF 2

3-9

3-10

	SEQUENTIAL CIRCUITS INC
TITLE	PCB 3 PARTS ID
SIZE	D
DWG No.	1000.3
DOCUMENT No.	PP331
SHEET	1 OF 1



NOTES:

1. U309 IS POWERED BY BT301 WHEN POWER SUPPLY IS OFF
2. VERSION Ø.V.8.2
3. VERSION 1.V.8.2
4. VERSION 2.V.8.2
5. MAY BE A JUMPER
6. MAY BE MOUNTED ON U320

LAST	NOT USED
BT301	
C386	
D319	
J302	
P304	
Q309	
R3153	
TP303	
U381	
W301	

DATE	REVISION
9/13/81	110 WAS V.81
7/8/80	29 C386 ADDED
	21 POWER DETECT

SEQUENTIAL CIRCUITS INC

TITLE: PCB 3 CPU, MEMORY, I/O INTFC

DSN: D — 1000.3

DWN: 4.22.80 — DOCUMENT NO: SD331

APP

ISS

SHEET 1 OF 4

3-11

DAC LOW BIT LATCH

DAC HIGH BIT LATCH

U336 14174 DBH0–DBH5 DBL0–DBL5 U329-10 CSOH6 U329-9 CSOH7

U337 14174

U342 4013 CLR

U343 4049

U344 4049

U345 4049

U346 DAC 71-CSB-I

(651μV) (1.302mV) (2.604mV) (5.208mV) (10.42mV) (20.83mV) (41.67mV) (83.33mV) (166.7mV) (333.3mV) (666.7mV) (1.333V) (2.667V) (5.333V)

+5V C355 2.2μF C360 2.2μF C323 C319 +15V R331 1K

0 LSB 15 MSB V REF NC GAIN ADJ COM C356 2.2μF -15V

DAC GAIN R329 100K 1% C359 .01μF R333 100K 20-TURN

R330 C358 I OUT RFB R330 332Ω 1% C358 120PF

DAC BUFFER U347 LF356 R332 5.62 R334 5K ADC GAIN R335 18.2K 1% R336 20.0K 1%

U364 TL082 1 STEP = 4mV (Vdac÷2)

Vdac GND → U355/56/57-3 P304 1 2

SPARES: 4049 ½U343 TL082 ½U364 LM339 ½U365

4 SOME UNITS ARE MODIFIED AS FOLLOWS TO ACCOMMODATE DACs WITH VOLTAGE OUTPUT (RATHER THAN CURRENT OUTPUT). THESE MODULES ARE MARKED "CSB-V" (RATHER THAN "CSB-I").

5 DATEL DACs HAVE PIN 18 REMOVED.

CASSETTE IN J9 BACK PANEL J11 P302 CASS IN

SEQ GATE IN J3 R315 100K R316 100K EXT GATE BUFFER

R311 100K C316 2ms DELAY FOR CV SLEW .02μ U330 4013 +CLR INT U319-10 CSOL5 U311-16 INT

C361 .02μF R337 4.99K 1% R341 10K 1% D305 IN914 R340 4.99K 1% R343 301K 1% R342 301K 1% R344 200K 1% R346 10M .93V .94V U365 LM339 CASS CPR R306 4.7K

J8 REL FT SW BACK PANEL

-EXT GATE EN DELAY FOR CV CONV ½U331 15V TO 5V LEVEL TRANSLATOR 74LS02 ½U321 U340-12 GATE 5 P304 60 S3 ENA REC

R317 4.7K P304 11 TUNE MUX

TUNE FF "FAKE" CLOCK 74LS74 ½U322 -FF CL

MISC LATCH -CSOL4 U319-11 U332 14174 DB0–DB5 FFP FFD CNTR EN RESET U311-26

R316 2K C315 R324 100K C351 .0056μF R323 22K

½U315 8253 COUNTER 0 CYCLE COUNTER (ONE SHOT) TUNE COUNTER

P302 J11 J10 C352 .1μF CASSETTE OUT

½U321 74LS02 C311 COUNTER 2 TOTAL TIME COUNTER 8253 ½U328 4504 440 P304 SEL 27

U325-9 2.5MHz A-440 24 COUNTER 1 A-440 DIVIDER 8253

FF STATUS

MISC INPUT BUS DRIVER U323 14503 U320-3 CSI1 R304 2K R312 100K R313 100K DB0 DB1 DB2 DB3 DB4 DB5

DBUS

ADC INPUT BUS DRIVER U324 14503 U320-8 CSI2 C312 R309 2K ADC LO ADC HI DB0 DB1 DB2 DB3 DB4 DB5

OSC SCALE TP301 R307 100K TP304 M TEST R355 100K TP306

ADC CPR R370 15K R371 5.62K 1% D307 IN914 R369 332Ω 1% R368 332Ω 1% R366 5.62K 1% R367 15K D306 IN914 R314 4.7K R305 4.7K ½U365 LM339

ADC +613mV ADC 0V ADC -606mV ADC -34mV ADC+ 34mV

SEQ OFFSET R385 100K R390 1M R389 1K ½U374 LM348 C374 C373 -8.6mV -3.7mV SEQ SCALE R392 24.9K 1% R396 10K R391 30.1K 1% D314 IN914 R396 470 -15V

J2 SEQ CV IN BACK PANEL J11 P302 U339-2 F EN SEQ CV

½U371 4016 R384 1K SEQ CV J302 Vmux

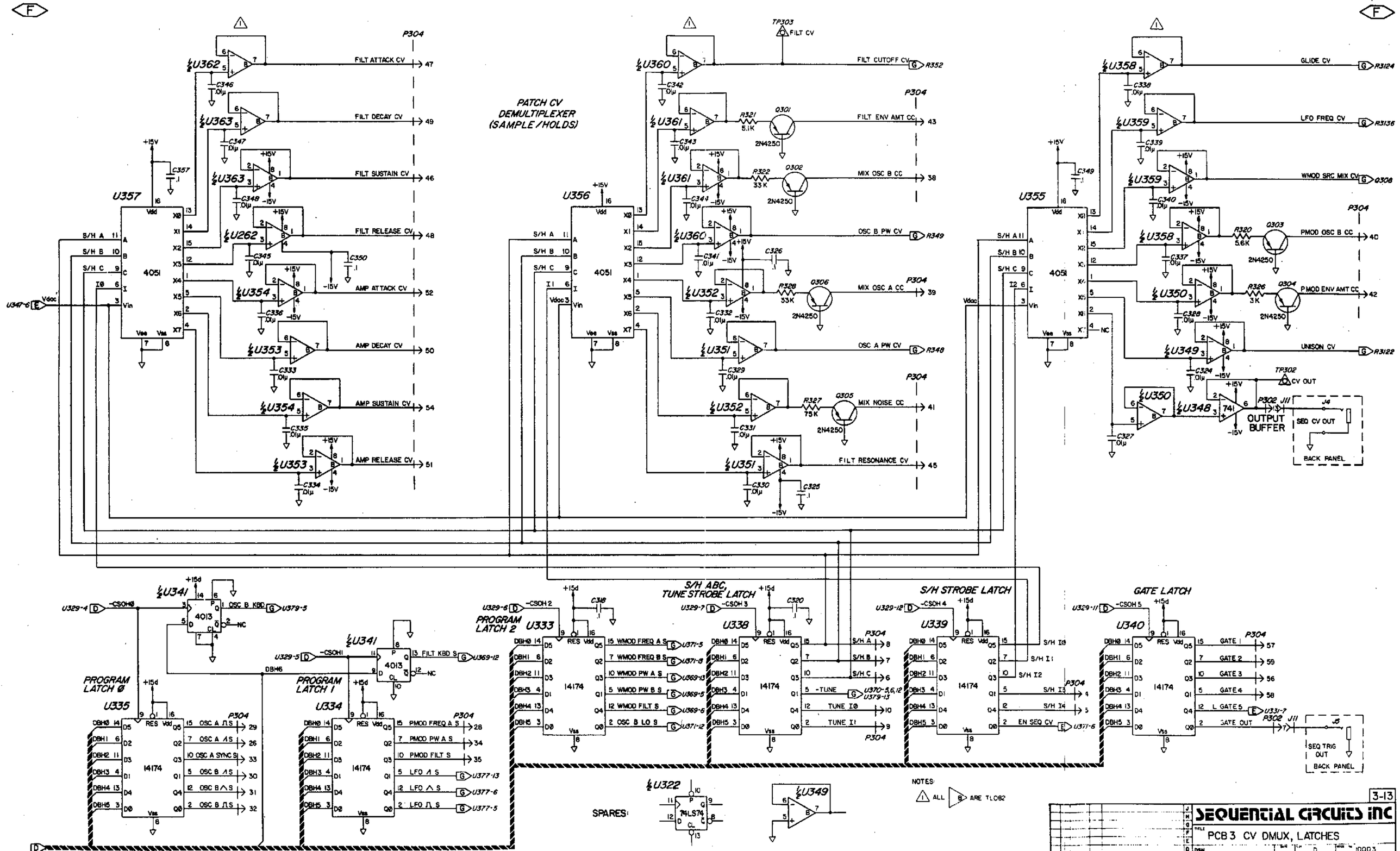
1 BIT EQUIVALENCIES

2 ONLY USED FOR OSC CVs

3 VOLTAGE READINGS WITH ALL POTS SET TO 0 AND U364-7 GROUNDED

3-12

J					SEQUENTIAL CIRCUITS INC
H					
G					
F					TITLE PCB 3 DAC, ADC, TUNE, SEQ, CASS
E					
D					DSN — SIZE D — DWG. No. 1000.3
C					DWN Jerry Anderson 1/11/80 — DOCUMENT No. SD332
B					APP
A					MFG S. Jerry Cobb 4/17/80 — SHEET 2 OF 4
130	5/7/80	20	EXTEND SEQ SCALE		
DWG. No.	DATE	ECN No.	REVISION		



SEQUENTIAL CIRCUITS INC

TITLE: PCB 3 CV DMUX, LATCHES

DBH | DWN | APP | ISS | REVISION | DATE

SIZE D | DWG # 10003 | DOCUMENT No SD333

J7 AMPLIFIER CV IN
BACK PANEL
J11 P301
R345 100
+5a
J302 P202 W201 W101
VOL IN
VOL OUT
P304
P401
VOL CV
R113 VOLUME 100K

+15V
R3106 4.7K
P301
J12
R1 PITCH WHEEL 100K
WHEEL PANEL
R3129 P-WH PITCH WHEEL TRIM 10K
NC
-15V

PW DEADBAND
D316 IN914
D315 IN914
R3100 100K 1%

U338-5 F -TUNE
R104 MASTER TUNE 100K
FRONT PANEL
P202 J302
R3102 100K 1%
D317 IN914
R377 1M 1%
R376 2.21M 1%
R378 100K 1% C368
½U370 4016
½U367 LM348

R3126 30K
Q309 A0820
U358-7 F GLIDE CV R3124 100K
R3125 2.7K
GLIDE
R3123 100K
U349-1 F UNISON CV R3122 4.7K
½U381 3280
D319 IN914
D318 IN914
½U380 TL082
C379
C376 1µF mylar 5%
C377
R3121 4.7K
NC

GLIDE OUT CV (UNI)

U375 5837
PINK NOISE SOURCE
R395 47K
R394 300K
R393 100K
C372 .01
R3116 8.2K
Q307
R3115 3.3K
2N4250
½U374 LM348
R3119 20K
½U378 3280
R3120 330
C378
NC
R3142 100K
NOISE BAL
R3144 200K
R3143 330

-600mV
D310 IN914
R388 1K
C369

U359-7 F LO FREQ CV
U359-1 F W MOD SRC MIX CV
LFO
U376
SUM
PW MOD
H SYNC
TCO
TCO
V-
LFM
HI FREQ GND
V+
3340
EXP CV
CF
S SYNC
R3135 887K 1%
R3110 10K
R3136 110K 1%
R3134 470
R3111 2K
C375 .01 mylar
R3112 470K
C385 .01
R3109 910
R3107 301K 1%
R3108 5.62K 1%
R3138 2.21M 1%
R3139 470
C384 .01
R3137 1.82K 1%
C382 .1 mylar 5%
C381
U334-5 F LFO Λ S
U334-2 F LFO Π S
U334-12 F LFO Λ S
C390
½U377 4016
R3133 160K
R3132 200K
R3127 10K
C383 .1
R3128 10K
Q308 2N4250
R3130 20K
R3146 10K
R3145 3.1K
R3149 1M
R3148 100K
R3147 100K
4.97V
2.47V
2.39V
½U380 TL082
R3131 160K
R3140 330
R3150 1M
R3141 100K
LFO BAL
R3151 2.2MΩ
R3152 330
½U378 3280
R3113 10K
R3114 3.3K

W-MOD SOURCE
P301
J12
R2 MOD WHEEL 100K
W-MOD BUFFER
½U374 LM348

SPARES:
J12/P301-4
½U379 4066
NC

U333-15 F WMOD FREQ A S
½U371 4016
W-MOD
R3104 182K 1%
D313 IN914
½U379 4066
R3117 1M
½U373 TL082
R382 100K 1%
R383 100K 1%
A OFFSET
R339 100K
R362 10M
R381 10K
½U368 LM348

U341-1 F OSC B KBD S
½U379 4066
½U373 TL082
R387 100K 1%
R3118 1M
U333-7 F WMOD FREQ B S
½U371 4016
R3103 182K 1%
D312 IN914
B OFFSET
R338 100K
R361 10M
R380 10K
½U368 LM348

U333-2 F OSC B LO FREQ S
½U371 4016
R3105 200K 1%

OSC A MSUM
R365 100K 1%
R364 100K 1%
R363 100K 1% C364 .01
½U368 LM348
A SUM
22

OSC B MSUM
R358 100K 1%
R359 100K 1%
R360 100K 1% C362 .01
½U368 LM348
B SUM
20

U341-13 F FILT KBD S
½U369 4016
FILTER CV IN BACK PANEL
J6 J11 P302
R374 100K 1%
R372 N 100K 1%
R354 N 100K 1%
C366
½U367 LM348
C367
R353 10K
R373 100K
½U366 LM348

U333-12 F WMOD FILT S
½U369 4016
R399 13.3K 1%
D311 IN914
U360-7 F FILT CTF CV R352 100K 1%
U333-5 F WMOD PW B S
½U369 4016
R398 15K
D309 IN914
U360-1 F OSC B PW CV R349 100K
U333-10 F WMOD PW A S
½U369 4016
R397 15K
D308 IN914
U351-7 F OSC A PW CV R348 100K
R347 100K

FILT MSUM
R357 N 100K 1% C365 .01
R356 261K 1%
R355 100K 1%
FILT SUM CV
14
PW B MSUM
R350 52.3K 1%
R351 100KΩ
PW B SUM CV
18
PW A MSUM
PW A SUM CV
16

A B N MATCHED TO .01%

SEQUENTIAL CIRCUITS INC
TITLE PCB 3 WMOD, MASTER SUMMERS
DWN
CHK D
APP
MFG S Langlois 9/14/82
DATE 8/11/82
DOCUMENT No. SD 334
SHEET 4 OF 4

SAMPLE AND HOLDS

U406 4051 — P401 S/H A, S/H B, S/H C, I3, Vdac (D401 1N914)
- ½U410 → OSC 1A S/H (I) R4321
- ½U410 → OSC 1B S/H (I) R4206
- U409 → OSC 2A S/H (J) R4328
- ½U410 → OSC 2B S/H (J) R4213
- ½U403 → OSC 3A S/H (K) R4335
- ½U404 → OSC 3B S/H (K) R4220
- ½U403 → OSC 4A S/H (L) R4342
- ½U404 → OSC 4B S/H (L) R4227

U405 4051 — P401 I4
- ½U408 → OSC 5A S/H (M) R4349
- U407 → OSC 5B S/H (M) R4234
- ½U408 → FILT 1 S/H (I) R4144
- ½U408 → FILT 2 S/H (J) R4148
- ½U401 → FILT 3 S/H (K) R4151
- U402 → FILT 4 S/H (L) R4153
- FILT 5 S/H (M) R4156

U439 4051
- U454-8 (I) OSC 1A Λ
- U441-8 (I) OSC 1B Λ
- U455-8 (J) OSC 2A Λ
- U442-8 (J) OSC 2B Λ
- U456-8 (K) OSC 3A Λ
- U443-8 (K) OSC 3B Λ
- U457-8 (L) OSC 4A Λ
- U444-8 (L) OSC 4B Λ

OSCILLATOR TUNING MULTIPLEXER
ONLY ACTIVE DURING TUNE

U440 4051
- U458-8 (M) OSC 5A Λ
- U445-8 (M) OSC 5B Λ

TUNE CPR
P401 TUNE I0 → U435 LM311 → P401 LF TUNE MUX
P401 TUNE I1

TO ALL AMP ENV GENs U412–U416
- P401 52 AMP ATK → R415 24.3K 1% → AAV (TM) pin 15
- R407 13K 1%, R402 806 1%
- 50 AMP DCY → R413 24.3K 1% → ADV (TM) pin 12
- R409 13K 1%, R404 806 1%
- 51 AMP REL → R414 24.3K 1% → ARV (TM) pin 13
- R408 13K 1%, R403 806 1%
- 54 AMP SUS → R405 4.75K 1% → ASV (TM) pin 9
- R406 4.75K 1%
- 47 FILT ATK → R410 24.3K 1% → FAV (TM) pin 18
- R427 13K 1%, R430 806 1%
- 49 FILT DCY → R412 24.3K 1% → FDV (TM) pin 12
- R429 13K 1%, R432 806 1%
- 48 FILT REL → R411 24.3K 1% → FRV (TM) pin 13
- R428 13K 1%, R431 806 1%
- 46 FILT SUS → R426 4.75K 1% → FSV (TM) pin 9
- R433 4.75K 1%

TO ALL FILT ENV GENs U417–U421

WHITE NOISE SOURCE
U427 5837 — C458, R4131 200K, C459 .1 -15V, B
U430 3080 — R4130 4.7K NOISE CV, R4152 10K, R4129 10K, NC, -15V
½U474 → NOISE (TM) R4367 R4376 R4385 R4394 R4403

U411 7905 — +15V, -15V, C423 10 10V, -5V

TB401 — J402 +15a, GND, -15a
- R4279 4.57V → TRI REF (TM) R4254 R4258 R4261 R4271 R4274
- R4290 4.99K 1%, C4105 2.2
- C421 10 25V, C422 10 25V
- R4182 780mV, 1K, D406 1N914, C471 .1, SWITCH REF
- I U436-7, M U437-7, L U438-7

U459 4016 — P401 A-440, A-440-SEL
U461 4016
U460 4016
- R4362 100K, R4356 1K, D418 1N914, C4140 .1
- TP401 A-440 → R4498 10K, R4519 20K, C4183 .1
- I U459-7, J U460-7, K U461-7, L U462-7, M U463-7

VOICE SUMMER
- U477-13 (I) VOICE 1 R4569 39K
- U477-12 (J) VOICE 2 R4568 39K
- U478-13 (K) VOICE 3 R4567 39K
- U478-12 (L) VOICE 4 R4566 39K
- U479-13 (M) VOICE 5 R4565 39K

½U480 — P401 VOLUME CV 44, R4535 100K, C4184 .22 tant.
½U480 — R4542 4.7K, Q411 2N4250, R4541 4.7K, R4561 68K
½U479 3080 — R4564 15K, R4553 13K, NC, -15V
C4189 non-polar, R4562 20K, R4543 100K

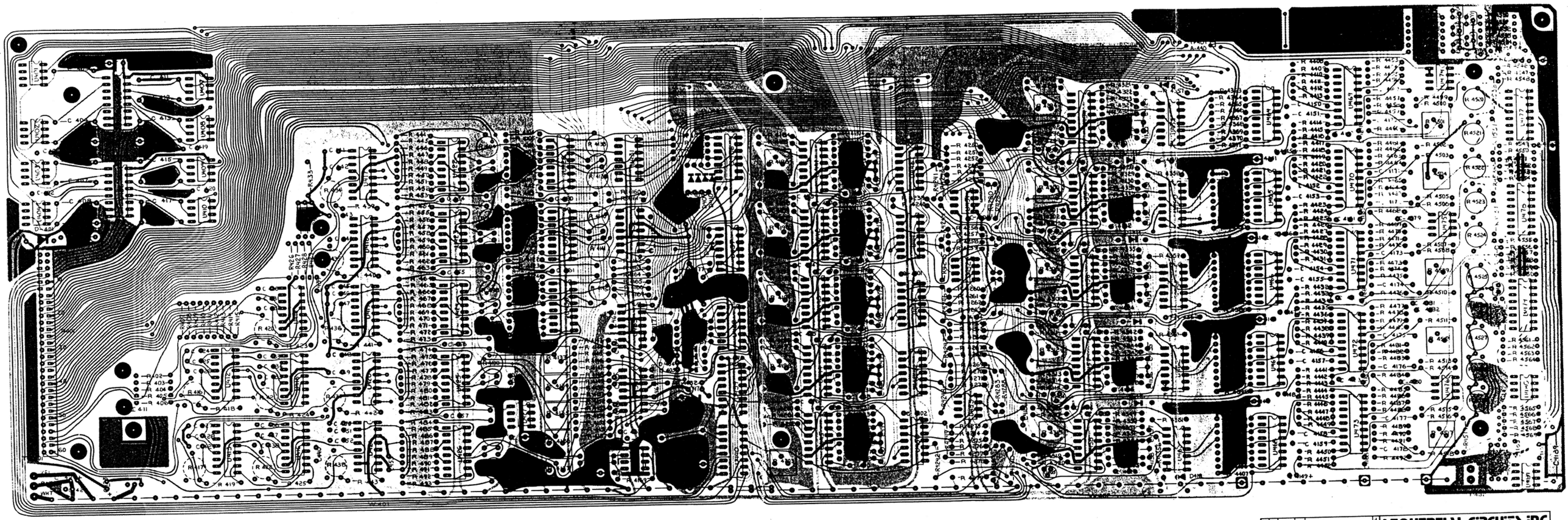
SPARES: ½U401, ½U451, ½U433 LM348, ½U437 4016, ½U462 4016, ½U463 4016 (-600mV)

U481 NE5534 — C4188, C4185
R4545 560, R4544 1K
P402 J14 → J1 AUDIO OUT (BACK PANEL)

LAST	NOT USED
C4189	
D418	
J402	J401
P402	
Q411	
R4569	R401/16,17/ 20-22/34-38
TB401	
U481	
W402	

1 ALL ½ B ARE TL082
2 ALL OIS/H CAPS ARE POLYSTYRENE
3 VOLTAGE READING WITH TUNE MUX INACTIVE.

SEQUENTIAL CIRCUITS INC
TITLE: PCB 4 CV DMUX, TUNE MUX, AUD OUT
DSN D — DWN 8/4/80 — APP — DATE D — MODEL NO. 1000.3 — DOCUMENT NO. SD430
8/6/80 B C458 .1 WAS 2.2
7/28/80 A R401 REMOVED
REVISION DATE BY
SHEET 1 OF 5
3-15



			SEQUENTIAL CIRCUITS INC	
			TITLE PCB 4 PARTS ID	
			DRN	DATE 1000.3
			DWN by Artist	4/4/84 DOCUMENT No PP431
			APP	
			ISS S. Taylor	9/13/84 SHEET 1 OF 1
LTR	DATE	ISS No	REVISION	

OSC A

OSC A PW SUMMER

OSC B

DC LEVEL-SHIFTER

PMOD BUFFER

FILTER

FINAL VCA

FILT FREQ SMR

AMP ENV GEN

FILT ENV GEN

△ RESISTORS MATCHED TO .01%

SEQUENTIAL CIRCUITS INC

PCB 4 VOICE I

DSN D 10003

DWN 6/16/80 SD431

APP

REVISION DATE

SHEET 2 OF

3-17

OSC A

OSC A PW SUMMER

OSC B

DC LEVEL-SHIFTER

PMOD BUFFER

FILTER

FINAL VCA

FILT FREQ SMR

AMP ENV GEN

FILT ENV GEN

△ RESISTORS MATCHED TO .01%

SEQUENTIAL CIRCUITS INC

PCB 4 VOICE 2

DSN

DWN

APP

ISS 5

DATE

REVISION

DOCUMENT No SD432

SHEET 3 OF

OSC A

OSC A PW SUMMER

OSC B

DC LEVEL-SHIFTER

PMOD BUFFER

FILTER

FINAL VCA

FILT FREQ SMR

AMP ENV GEN

FILT ENV GEN

△ RESISTORS MATCHED TO .01%

SEQUENTIAL CIRCUITS INC

PCB 4 VOICE 3

1000.3

SD433

SHEET 4 OF

OSC A

OSC A PW SUMMER

OSC B

DC LEVEL-SHIFTER

PMOD BUFFER

FILTER

FINAL VCA

FILT FREQ SMR

AMP ENV GEN

FILT ENV GEN

RESISTORS MATCHED TO .01%

3-20

SEQUENTIAL CIRCUITS INC

PCB 4 VOICE 4

SD434

SHEET 5 OF

M

OSC A
OSC A PW SUMMER
OSC B
OC LEVEL-SHIFTER
PMOD BUFFER
FILTER
FILT FREQ SMR
FINAL VCA
AMP ENV GEN
FILT ENV GEN

△ RESISTORS MATCHED TO .01%

SEQUENTIAL CIRCUITS INC

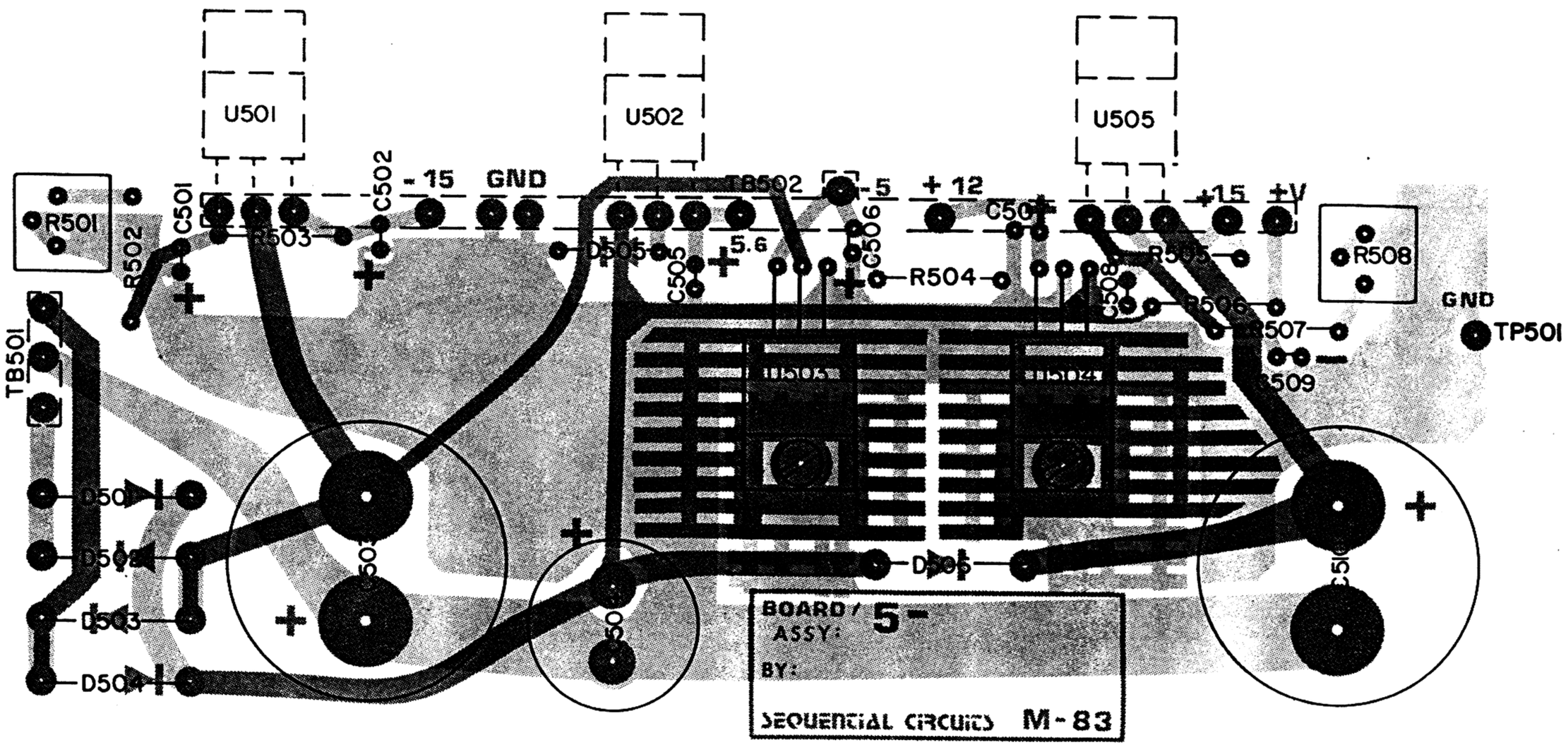
PCB 4 VOICE 5

DSN D 1000.3

DWN Greg Ambert 8/1/80 DOCUMENT No SD435

APP

REVISION DATE 1/14/80 SHEET 6 OF

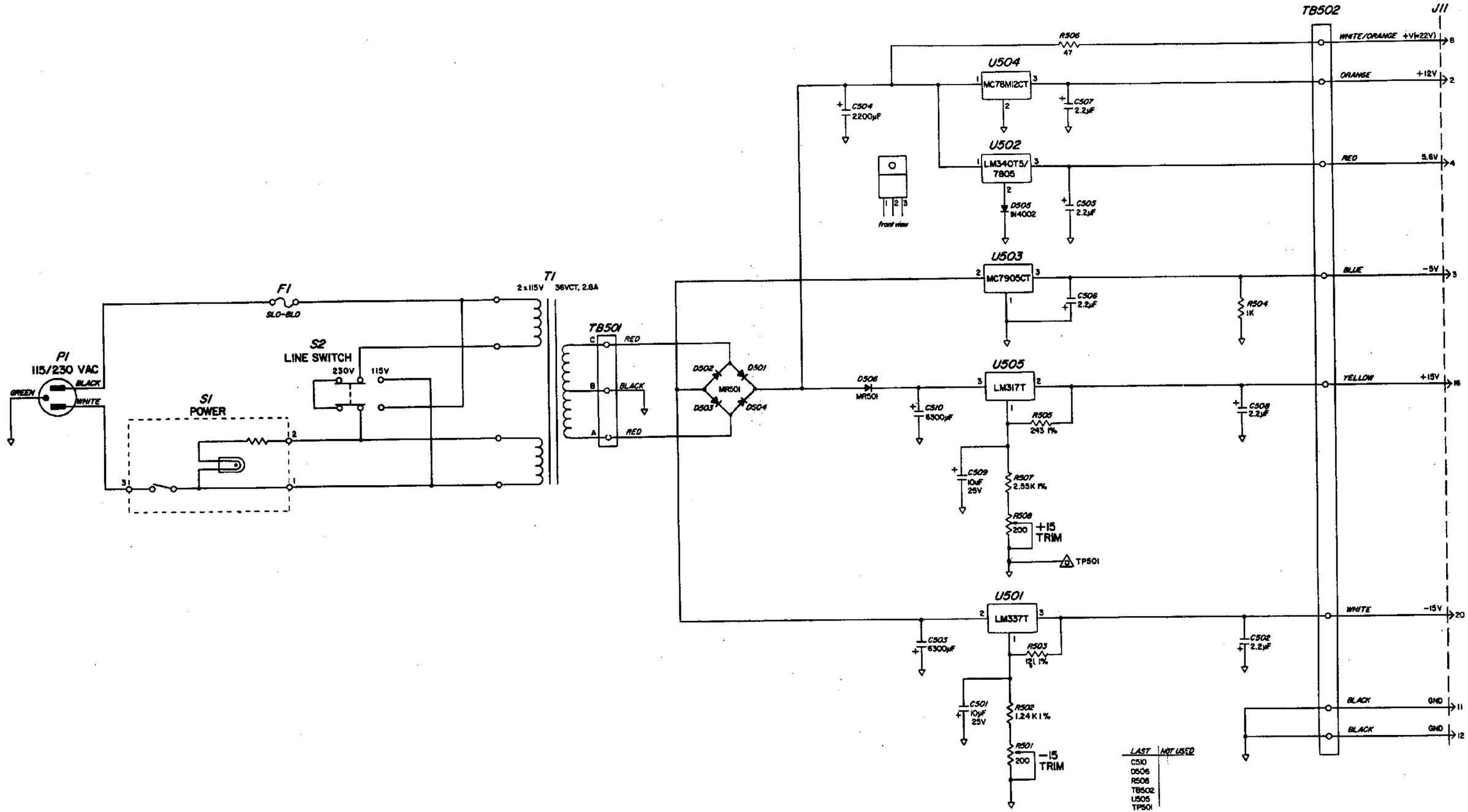


					J
					H
					G
					F
					E
					D
					C
					B
		10/21/80	36	Remove +12 & -5 circuits	A
FIRST / LAST S/N		DATE	ECR No	REVISION	LTR

SEQUENTIAL CIRCUITS INC

TITLE: PCB 5 PARTS ID

DSN	DATE	SIZE B	MODEL No 1000.3
DWG D. SIMARD		DOCUMENT No PP531	
APP			
ISS S Armstrong	9/12/80		SHEET 1 OF 1



3-23/3-24

SEQUENTIAL CIRCUITS INC

PCB 5 POWER SUPPLY

DRN

APP

REVISION

SIZE D

1000.3

DOCUMENT No. SD531

SHEET 1 OF 1

SECTION 4
SERVICE

4-0 GENERAL

This section contains detailed service instructions for complete functional testing and for all adjustments. Instruments to be serviced should be thoroughly tested beforehand. This will verify a malfunction has indeed occured, perhaps reveal related or unrelated malfunctions, and provide a basis for troubleshooting. The tests suggest trims which may restore normal functions. If the problem(s) persist, you will have to rely on Sections 2 and 3 and your troubleshooting skills to locate the defective component(s).

Throughout the functional tests you must play five different keys to test the five individual voices. All tests are performed by ear; the object generally being consistency between the voices. There will always be slight variations between the voices. If not excessive these differences help to "warm" the Prophet's sound.

Note that while all tests can be performed with the cabinet unopened you will have to open the cabinet to identify the individual voices since there is no reliable way of identifying them by merely listening. To check a single voice, its GATE or Final VCA output can be probed, or its relative volume manipulated (see paragraph 4-22). You may also be able to use the fact that the first voice assigned after the TUNE routine is Voice 1.

Prophet trimming is a sensitive procedure which as a rule should not be done more than necessary. Prophets are carefully adjusted at the factory, where many trimmers are sealed to prevent misadjustment by vibration or accident. You will rarely be able to make an audible improvement upon these trims—unless a malfunction has occured or a part has been replaced. If you do try to ideally set all 54 trimmers when no repairs have been involved, you may succeed only in correcting for the difference between our DVMs or room temperature and yours.

Most trims require a 4-1/2 digit DVM. An oscilloscope (preferably, dual-trace) is required for filter tuning and for serious troubleshooting.

These procedures are presented in the order recommended for a Prophet assumed to be 100% electrically functional but untrimmed. Real-world problems may require you change the order of some tests and adjustments. Therefore each procedure is written to be performed independently of the others.

In preparation for service, set up the Prophet as follows:

1. Connect mono phone-plug between back panel AUDIO OUT jack and power amplifier.
2. Check back panel 115/230 line voltage selector.
3. Check that back panel power switch is off.
4. Connect power cord to properly-grounded outlet.
5. Switch power on. The power switch should light. TUNE switch on control panel will initially light. After ten seconds, PRESET mode and BANK-PROGRAM 1-1 "comes up." If not, check fuse: 115V—3/4A SLO BLO; 230V—1/2A SLO BLO.
6. Center PITCH wheel and set MOD wheel to minimum.
7. To be safe, SAVE the current program file through the CASSETTE interface. (Better yet, insist owners "back-up" before delivering the machine for service.)
8. Set back panel RECORD ENABLE/DISABLE switch to DISABLE to protect NV RAM.
9. Adjust VOLUME as required.

See Section 1 for mechanical procedures required for service. Sealent can be easily pulled off of trimmers with needle-nose pliers. Be sure to reseal any trim setting you change. It is customary to install sockets when replacing soldered ICs. Also note that the Prophet presets to 1-1 whenever power is switched on. This means you may have to check the controls whenever you power up—after swinging out PCB 4, for example.

IMPORTANT! WHENEVER THE AUDIO CABLE IS DISCONNECTED, PCB 3 MUST BE GROUNDED TO THE BACK PANEL.

4-1 OSCILLATOR A TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-1.
2	—	TUNE	ON	WHEN DONE, PLAY HIGHEST KEY (C5) AND REMEMBER PITCH.
3	OSC A	FREQ	10	HOLD SECOND C (C1) FROM BOTTOM (C0). SAME PITCH AS STEP 2.
4	OSC A	FREQ	0-10	PITCH ADJUSTS IN SEMITONES OVER 4-OCTAVE RANGE. CHECK THAT EACH OSC PLAYS IN TUNE OVER FULL 9-OCTAVE RANGE.
5	OSC A	SYNC	ON	
6	OSC B	KBD	ON	
7	OSC A	FREQ	0-10	SYNC FUNCTION
8	OSC A	FREQ	4	NORMAL KEYBOARD RANGE
9	OSC B	KBD	OFF	
10	OSC A	SYNC	OFF	
11	OSC A	SAW	OFF	
12	OSC A	PULSE	ON	
13	OSC A	PW	0-10	PULSE DEGENERATES NEAR SAME EXTREME KNOB SETTINGS FOR ALL VOICES.

RELATED TRIMS: 4-14 DAC GAIN, ADC GAIN, SEQ INTERFACE
4-16 VCO SCALE

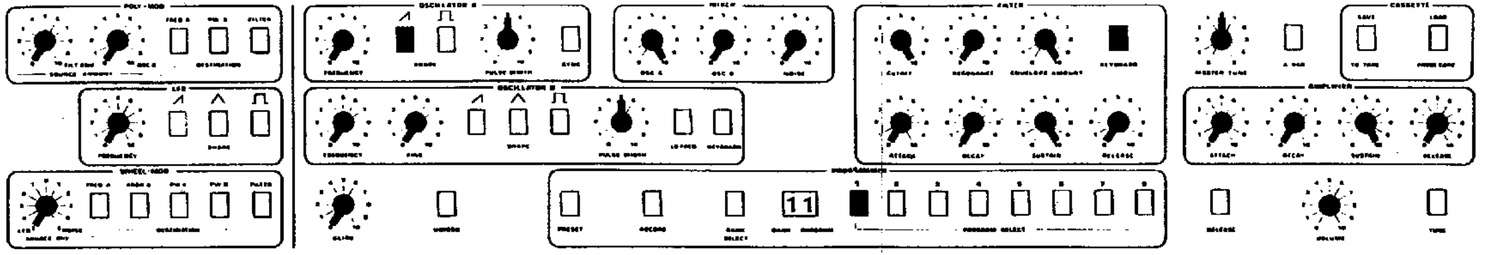


Figure 4-1
OSC A TEST PATCH

4-2 OSCILLATOR B TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-2.
2	—	TUNE	ON	WHEN DONE, PLAY HIGHEST KEY (C5) AND REMEMBER PITCH
3	OSC B	FREQ	10	HOLD SECOND C (C1) FROM BOTTOM (C0). SAME PITCH AS STEP 2.
4	OSC B	FREQ	0-10	PITCH ADJUSTS IN SEMITONES OVER 4-OCTAVE RANGE
5	OSC B	FREQ	4	
6	OSC B	FINE	0-10	PITCH ADJUSTS CONTINUOUSLY OVER 1-SEMITONE RANGE.
7	OSC B	FINE	0	
8	OSC B	SAW	OFF	
9	OSC B	TRI	ON	DULLER TIMBRE, FREE OF HARMONICS.
10	OSC B	TRI	OFF	
11	OSC B	PULSE	ON	
12	OSC B	PW	0-10	PULSE DEGENERATES NEAR SAME EXTREME KNOB SETTINGS FOR ALL VOICES.
13	OSC B	PW	5	
14	OSC B	PULSE	OFF	
15	OSC B	SAW	ON	
16	OSC B	LO FREQ	ON	
17	OSC B	FREQ	0-5	2-40 HZ, CONTROLLED BY HIGHEST KEYS (C3-C5)
18	OSC B	KBD	OFF	
19	OSC B	FREQ	0-10	.1-40 HZ, FIXED FREQ. SLIGHT VARIATION BETWEEN VOICES.

RELATED TRIMS: 4-14 DAC GAIN, ADC GAIN, SEQ INTERFACE TRIM
4-16 VCO SCALE

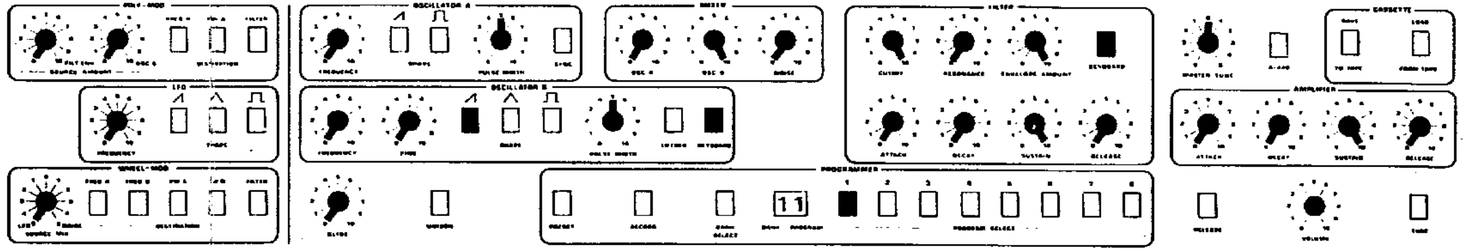


Figure 4-2
OSC B TEST PATCH

4-3 MIXER AND NOISE TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-3.
2	MIX	OSC A	0-10	SMOOTH LEVEL CONTROL THROUGHOUT RANGE. VOICES STAY IN BALANCE.
3	MIX	OSC A	0	
4	MIX	OSC B	0-10	SAME AS STEP 2
5	MIX	OSC B	0	
6	MIX	NOISE	0-10	SAME AS STEP 2

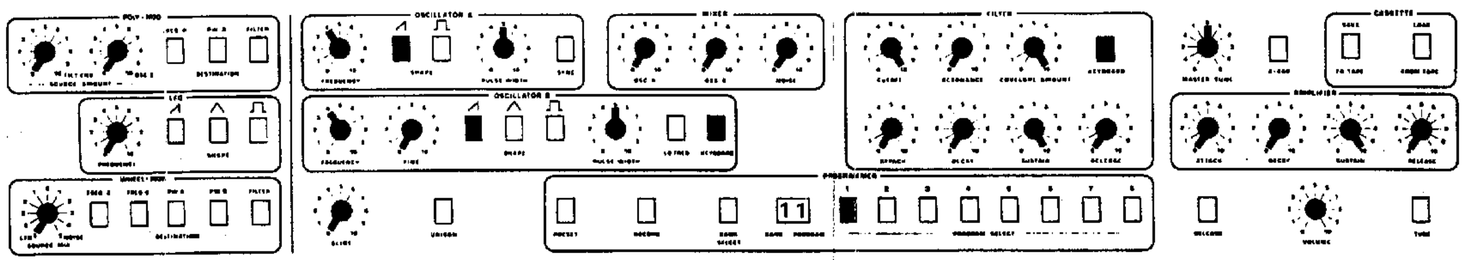


Figure 4-3
MIXER AND NOISE TEST PATCH

4-4 UNISON AND GLIDE TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-4.
2	—	TUNE	ON	WHEN DONE, CHECK THAT OSC A AND OSC B FREQ ARE BOTH SET UP TWO OCTAVES (FROM 0).
3	OSC A OSC B	FREQ FREQ	4 4	
4	—	A-440	ON	440 REFERENCE ON
5	—	MTUN	+/–1	FINE-TUNE FOR ZERO-BEAT. RESET OSC A AND OSC B FREQ IF REQUIRED.
6	—	A-440	OFF	
7	WHEEL	PITCH	U/D	RAISES AND LOWERS PITCH BY AT LEAST A FIFTH. OSC A AND OSC B MUST TRACK.
8	—	UNI	ON	
9	WHEEL	PITCH	U/D	SAME AS STEP 7
10	WHEEL	PITCH	CENTER	HOLD C5 AND PLAY C0. NO GLIDE.
11	—	GLIDE	6	MEDIUM GLIDE.
12	—	GLIDE	10	MINIMUM: 5 SECS TO SLEW 5 OCTAVES.
13	—	UNI	OFF	
14	—	GLIDE	0-10	NO DETUNING OF OSC A OR OSC B.

RELATED TRIMS: 4-11 PITCH WHEEL
4-16 VCO SCALE

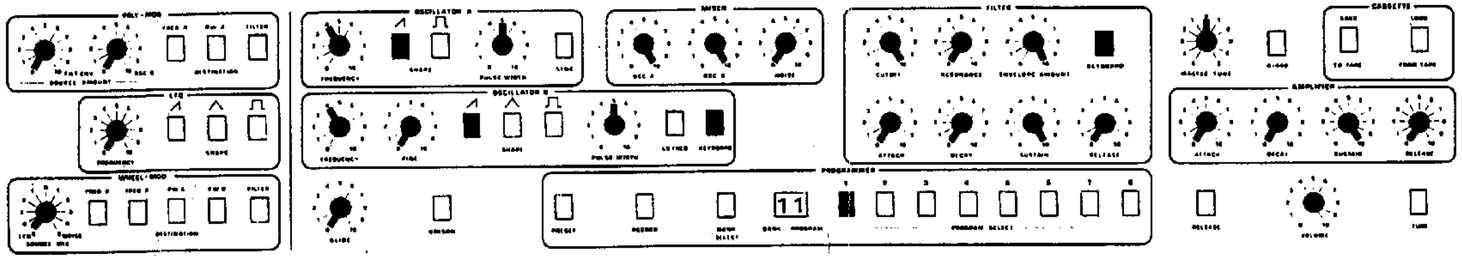


Figure 4-4
UNISON AND GLIDE TEST PATCH

4-5 FILTER TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-5.
2	FILT	CTF	0-10	SINE-WAVE OSCILLATION THROUGH RANGE.
3	FILT	CTF	4	NORMAL KEYBOARD RANGE.
4	FILT	ENV AMT	0-10	DOESN'T DETUNE ANY VOICE.
5	FILT	KBD	ON/OFF	KEYBOARD TRACKING.
6	FILT	ENV AMT	4	
7	FILT	KBD	ON	
8	FILT	RES	0-10	ALL FILTERS OSCILLATE BETWEEN 7 AND 9-1/2 ON DIAL AND WITHIN 1-1/2 MARKS OF EACH OTHER.
9	FILT	RES	10	
10	FILT	ATK	6	APPROX 1-SEC ATTACK
11	FILT	ATK	0	
12	FILT	DEC	6	APPROX 1-SEC DECAY
13	FILT	DEC	0	
14	FILT	SUS	0-10	RAISES FREQS EVENLY
15	FILT	SUS	10	
16	FILT	REL	6	SWITCH RELEASE ON AND BACK OFF TO KILL DRONING AMP.
18	FILT	REL	10	GREATER THAN 20-SEC RELEASE

RELATED TRIMS: 4-19 FILTER ENVELOPE AMOUNT VCA
4-20 FILTER TUNING

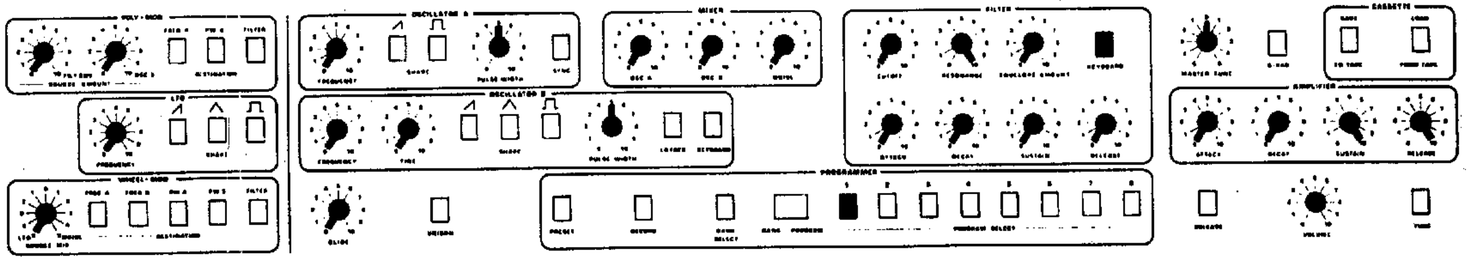


Figure 4-5
FILTER TEST PATCH

4-6 AMPLIFIER TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-6.
2				1-SEC ATTACK
3	AMP	ATK	0	
4	AMP	DEC	6	1-SEC DELAY
5	AMP	DEC	0	
6	AMP	SUS	0-10	SMOOTH VOL INCREASE
7	AMP	SUS	10	
8	AMP	REL	6	1-SEC RELEASE
9	AMP	REL	10	GREATER THAN 20-SEC RELEASE.

RELATED TRIMS: 4-21 FINAL VCA BALANCE
NOTE. THIS TRIM IS INDICATED IF A THUMPING IS HEARD DURING THE TEST.
4-22 VOICE VOLUME

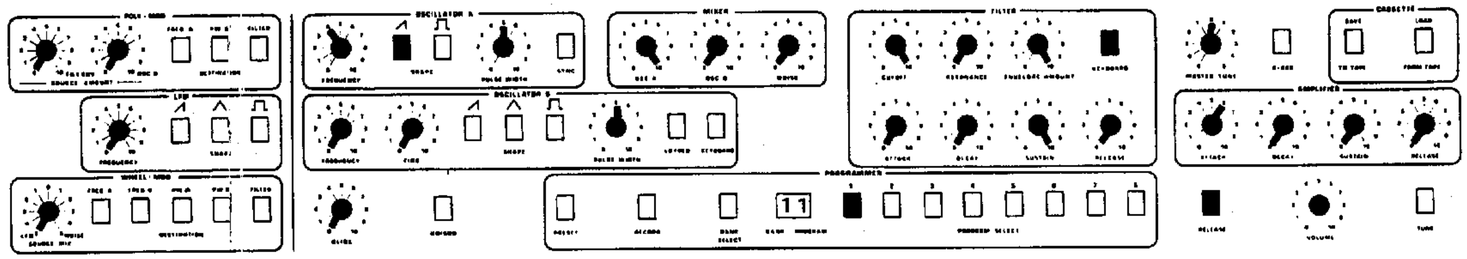


Figure 4-6
AMPLIFIER TEST PATCH

4-7 LFO AND WHEEL-MOD TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-7.
2	W-MOD	FREQ B	ON/OFF	NO OFFSET **(LEAVE OFF)**
3	W-MOD	FREQ A	ON/OFF	NO OFFSET
4	W-MOD	FREQ A	ON	
5	WHEEL	MOD	UP	NO OFFSET. MOVE MOD WHEEL UP AND DOWN THROUGHOUT REST OF TEST.
6	LFO	TRI	ON	SMOOTH CONTROL
7	LFO	FREQ	0-10	
8	LFO	FREQ	6	
9	LFO	TRI	OFF	
10	LFO	SQUARE	ON	50% DUTY CYCLE, INCREASING INTERVAL WITH INCREASED MOD-WHEEL SETTING.
11	LFO	SQUARE	OFF	
12	LFO	SAW	ON	SMOOTH RAMP
13	LFO	FREQ	3	SLOW, SMOOTH RAMP
14	LFO	FREQ	7	FASTER RAMP
15	LFO	SAW	OFF	
16	LFO	TRI	ON	
17	W-MOD	FREQ A	OFF	
18	W-MOD	PW A	ON	PW-MOD
19	W-MOD	PW A	OFF	
20	W-MOD	FILT	ON	FILT- **MOD**
21	W-MOD	FILT	OFF	
22	OSC A	PULSE	OFF	
23	OSC B	PULSE	ON	
24	W-MOD	PW B	ON	
25	W-MOD	PW B	OFF	
26	W-MOD	FREQ B	ON	
27	LFO	TRI	OFF	
28	W-MOD	SRC MIX	NOISE	NO OFFSET

RELATED TRIMS: 4-12 MASTER SUMMER OFFSET
4-13 WHEEL—MOD LFO VCA BALANCE
4-15 WHEEL-MOD NOISE VCA BALANCE

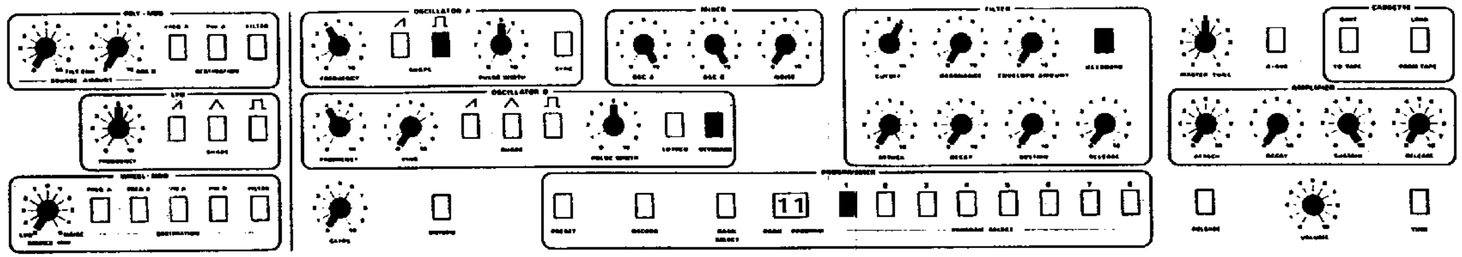


Figure 4-7
LFO AND WHEEL-MOD TEST PATCH

4-8 POLY-MOD TEST

STEP	MODULE	CONTROL	SETTING	NORMAL INDICATIONS/COMMENTS
1	PRGMR	PRST	OFF	SET CONTROLS ACCORDING TO FIGURE 4-8.
2	P-MOD	FREQ A	ON/OFF	NO OFFSET **(LEAVE OFF)**
3	P-MOD	PW A	ON/OFF	NO OFFSET **(LEAVE OFF)**
4	P-MOD	FILT	ON/OFF	NO OFFSET **(LEAVE OFF)**
5	P-MOD	FREQ A	ON	
6	P-MOD	FIL ENV	0-10	NO OFFSET
7	P-MOD	ENV	0	
8	P-MOD	OSC B	0-10	NO OFFSET
9	P-MOD	OSC B	0	
10	FILT	DEC	5	
11	OSC B	TRI	ON	
12	P-MOD	FIL ENV	2	DESCENDING FREQ
13	P-MOD	FIL ENV	4	DESCENDING FREQ
14	P-MOD	FIL ENV	10	SIMILAR
15	P-MOD	FIL ENV	0	
16	P-MOD	OSC B	4	MOD
17	P-MOD	OSC B	10	SIMILAR
18	P-MOD	OSC B	0	
19	P-MOD	FREQ A	OFF	
20	P-MOD	PW A	**ON**	
21	OSC A	PW	2	
22	P-MOD	FIL ENV	4	**PW-SWEEP**
23	P-MOD	FIL ENV	10	
24	P-MOD	FIL ENV	0	
25	P-MOD	OSC B	4	**MOD**
26	P-MOD	OSC B	10	
27	P-MOD	OSC B	0	
28	P-MOD	PW A	OFF	
29	P-MOD	FILT	ON	
30	OSC A	PULSE	OFF	
31	FILT	CTF	4	
32	FILT	RES	10	
33	P-MOD	FIL ENV	4	DESCENDING RES FILT SWEEP
34	P-MOD	FIL ENV	10	SIMILAR
35	P-MOD	FIL ENV	0	
36	P-MOD	OSC B	4	MOD
37	P-MOD	OSC B	10	
38	P-MOD	OSC B	0	

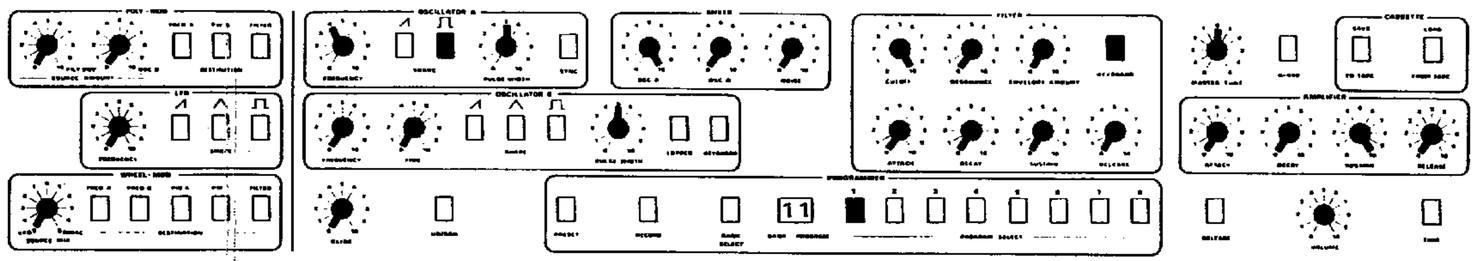


Figure 4-8
POLY-MOD TEST PATCH

RELATED TRIMS: 4-17 POLY-MOD FILTER ENVELOPE VCA BALANCE
4-18 POLY-MOD OSCILLATOR B VCA BALANCE

4-9 FINAL TEST

1. Check that the back panel RECORD switch is DISABLEd.
2. Press RECORD. It should not light.
3. If necessary, load custom or factory programs through the Cassette Interface.
4. Select a program.
5. Patch SEQUENCER VOLTAGE OUT jack to FILTER CONTROL VOLTAGE IN and check for increased brightness across entire keyboard.
6. Move connector from FILTER CONTROL VOLTAGE IN to AMPLIFIER CONTROL VOLTAGE IN. Volume should increase as you play up from the bottom of the keyboard.
7. Move connector from AMPLIFIER CONTROL VOLTAGE IN to SEQUENCER VOLTAGE IN.
8. Patch SEQUENCER TRIGGER OUT to SEQUENCER GATE IN. Check for function and offset.
9. Remove both SEQUENCER INTERFACE cords.
10. Connect footswitch to RELEASE FOOTSWITCH jack.
11. With factory program 1-4 or similar selected, play and check for footswitch function. (Switch RELEASE off.)

RELATED TRIMS: 4-14 DAC GAIN, ADC GAIN, AND SEQ INTERFACE
4-21 FINAL VCA BALANCE
4-22 VOICE VOLUME

4-10 POWER SUPPLY TRIM

GENERALLY, THE POWER SUPPLY SHOULD NOT BE ADJUSTED UNLESS IT HAS BEEN REPAIRED, READJUSTMENT WILL OFFSET ALL OTA BALANCES, WHICH WILL THEN HAVE TO BE RE-TRIMMED.

1. With power off, unscrew the box and slide the top panel assembly forward as discussed in paragraph 1-2, but do not raise to service position.
2. For component location see PP531. For schematic, see SD531.
3. Switch power on.
4. Probe +15V where marked on PCB 5 and adjust R508 to read +15.000V.
5. Probe -15 where marked on PCB 5 and adjust R501 to read -15.000V.
6. Repeat steps 4 and 5 as required. (It is probably not possible to make these settings perfect.)

TO TRIM, THE SUPPLY MUST BE FULLY LOADED.

AFTER REPAIR, CHECK POWER SUPPLY OUTPUT BEFORE INSTALLING, BUT DO NOT OPERATE THE UNLOADED SUPPLY FOR LONG PERIODS WITHOUT HEAT-SINKING THE REGULATORS. NEVER OPERATE THE SUPPLY UNDER LOAD WITHOUT HEATSINKING.

WHEN INSTALLING, BE SURE REGULATOR TABS ARE FLAT AGAINST THE HEATSINK AND THE MICA INSULATOR IS WELL-COATED ON BOTH SIDES WITH THERMAL COMPOUND. BEFORE APPLYING POWER, CHECK REGULATOR INSULATION FROM BACK PANEL WITH OHMETER. ALL OUTPUTS SHOULD READ "INFINITE" RESISTANCE.

4-11 PITCH WHEEL TRIM

This trim removes offset from the pitch wheel, so that when centered, R1 adds .0000V to the master summers. Trimming R3129 may only be required. For complete pitch-wheel alignment:

1. Switch power off and swingout PCB 4. (Be sure to ground PCB 3.)
2. Switch power on.
3. For component locations, see PP331. For schematic see SD334.
4. Probe P301-7 with DVM.
5. Center R3129 P-WH trimmer.
6. Loosen pitch wheel set screw. For location, see Figure 1-4.
7. With your left hand, hold the pitch wheel tight by pressing the detent with your thumb while pushing against the exposed center notch with your second finger.
8. While holding the wheel steady, adjust R1 to read +/- .05V by turning the shaft slot—rather than the wheel.
9. Being certain the wheel is center-detented, tighten set screw.
10. Move wheel up and down and check center-detent position reads +/- .05V.
11. Trim-out residual offset with R3129.
12. Repeat steps 10 and 11 for best repeatability of .000-V reading.

4-12 MASTER SUMMER OFFSET TRIM

The A and B OFFSET trimmers remove residual wheel-mod offsets in the Master Summers.

1. Switch power off and swing-out PCB 4.
2. Switch power on.
3. For component locations see PP331. For schematic, see SD334.
4. Check that R2 MOD wheel is set to minimum.
5. Probe U368-7 by clipping to the left end of R363.
6. Toggle W-MOD FREQ A switch and adjust R339 A OFFSET for same reading (e.g. +/- mV) with W-MOD FREQ A on and off.
7. Probe U368-1 by clipping on to the left end of R360.
8. Toggle W-MOD FREQ B and adjust R338 B OFFSET as in step 6.

4-13 WHEEL-MOD LFO VCA BALANCE

1. Switch power off and unmount PCB 4.
2. For component locations see PP331. For schematic, see SD334.
3. Check that W-MOD SRC MIX is set to LFO and all W-MOD DESTINATIONS and LFO SHAPEs are off.
4. Probe U378-13 by clipping on to left end of R3113.
5. Trim R3141 LFO BAL to read 0.000V.

4-14 DAC GAIN, ADC GAIN, SEQ INTERFACE TRIM

This procedure actually contains four trims which need always be performed together and in the order given.

1. Switch power off and unmount PCB 4.
2. For component locations see PP331. For schematic, see SD332 and SD333.
3. Hit C0 (lowest key).
4. Probe U348-6 at TP302 CV OUT hole and note reading (e.g., +0.093V).
5. Hit C5 (highest key).
6. Trim R333 DAC GAIN for reading in step 4 plus exactly 5.000V (e.g., +5.093V).
7. Repeat steps 3 - 6 until exact.
8. Check other Cs. Each should be exact (e.g., 1.093, 2.093...).
9. Set FILT CUTOFF knob to 10.
10. Probe U360-7 at TP303 FILT CV hole just above U350.
11. Trim R334 ADC GAIN to read as close to 10.000V as the 83-mV quantized voltage steps will allow.
12. Patch SEQ VOLTAGE OUT to SEQUENCER VOLTAGE IN and SEQUENCER TRIGGER OUT to SEQ GATE IN.
13. Probe U374-1, by clipping to right end of R389.
14. Hit C0.
15. Trim R385 SEQ OFFSET reading to exactly half that read in step 4 (e.g. 0.093/2 = 0.046).
16. Select a non-UNISON program. While playing monophonically, trim R386 SEQ SCALE so Voice 5 plays the same note as the other voice over the entire keyboard. (Hit key repeatedly while trimming.).
17. Disconnect sequencer interface cables.

4-15 WHEEL-MOD NOISE VCA BALANCE

PCB 4 need not be removed for this trim.

1. Switch PRESET off and set up controls according to Figure 4-4.
2. Turn W-MOD SRC MIX to NOISE.
3. Switch W-MOD FREQ B on.
4. Press TUNE. When done tuning, zero-beat oscillators (Leave OSC B FINE at 0).
5. With your left hand, play a key while advancing the MOD wheel until beating is heard.
6. R3142 NOISE BALANCE is accessible through a hole on PCB 4 near U418. Trim out beats.

4-16 VCO SCALE TRIM

BE SURE RECORD IS DISABLED

THE RANGE OF THE TUNE SYSTEM IS LARGE ENOUGH SO IT WILL RARELY BE NECESSARY TO TRIM VCO SCALE. IN FACT VCOS CAN USUALLY BE SUBSTITUTED WITHOUT ANY READJUSTMENT. THEREFORE IF THE PROPHET IS BADLY OUT OF TUNE THERE IS PROBABLY A COMPONENT FAILURE.

A SCALE TRIM IS INDICATED FOR OSCILLATORS WHICH DO NOT TRACK THE PITCH WHEEL, OR WHICH ARE DETUNED IN UNISON, ESPECIALLY WITH LONG GLIDE TIMES.

This trim uses a special microcomputer subroutine which sets up the VCOs to be scaled in the order OSC 1A, 1B, 2A, 2B, 3A, etc. The lowest key, C0, is used to tell the microcomputer to recompute the VCO SCALE bias. One starts with OSC 1A by trimming for zero-beat with a C-reference which the computer also provides (through the A-440 circuit), hitting C0, retrimming, hitting C0, and retrimming and so on until no further improvement can be made. Then key D0 is pressed to bring up the next oscillator, 1B, and the process repeated (trim, C0, trim, C0, etc.).

1. Locate TP301 at U324-6 (schematic SD332). Tie this to +5V (Most PCB 3s have a wire loop at the +5V rail, left of U301 - U308).
2. Press TUNE. You will now hear OSC 1A's sawtooth with a reference tone in the background.
3. Trim R4294 OSC 1A SCALE for zero-beat. Hit key C0 and retrim, using a good amount of "overshoot." Repeat until the tones are in zero-beat.
4. When OSC 1A is done, hit key D0 and TRIM OSC 1B. Table 4-0 lists OSC SCALE trim designators.
5. Repeat step 4 for OSC 2A - 5B. If you lose track of which VCO you are supposed to be trimming, simply run your hand along the two rows of VCOs (see Figure 1-0). You will know when you touch a pin of the currently-tuning VCO—they are very sensitive to detuning in this way.
6. When done untie TP301 from +5V. The Prophet will enter TUNE mode, then come up to program 1-1.

Table 4-0
OSCILLATOR SCALE TRIMMERS

VCO	TRIMMER
1A	R4294
1B	R4186
2A	R4300
2B	R4190
3A	R4306
3B	R4194
4A	R4312
4B	R4198
5A	R4318
5B	R4203

4-17 POLY-MOD FILTER ENVELOPE VCA BALANCE

1. Switch PRESET off and set controls according to Figure 4-8.
2. To trim Voice 1, first turn P-MOD FILT ENV to 10.
3. Probe U422-13 by clipping to right end of R4108.
4. With no keys hit, trim R494 for .000V.
5. Trim Voices 2 - 5 in the same way, referring to Table 4-1.

Table 4-1
POLY-MOD FILTER ENVELOPE VCA BALANCE

VOICE	OTA	PROBE (RIGHT END)	TRIMMER
1	U422-13	R4108	R494
2	U423-13	R4109	R496
3	U424-13	R4118	R498
4	U425-13	R4119	R4100
5	U426-13	R4128	R4102

4-18 POLY-MOD OSCILLATOR B VCA BALANCE

1. Switch PRESET off and set controls according to Figure 4-8.
2. Turn P-MOD OSC B to 10.
3. Probe U428-13 by clipping to right end of R4108.
4. With no keys hit, trim R4138 for .000V.
5. Trim Voices 2 - 5 in the same way, referring to Table 4-2.

Table 4-2
POLY MOD OSC B VCA BALANCE

VOICE	OTA	PROBE (RIGHT END)	TRIMMER
1	U428-13	R4108	R4138
2	U428-12	R4109	R4139
3	U429-13	R4118	R4140
4	U429-12	R4119	R4141
5	U430-13	R4128	R4142

4-19 FILTER ENVELOPE AMOUNT VCA BALANCE

1. Switch PRESET off and set controls according to Figure 4-8.
2. Switch FILTER KEYBOARD off.
3. Probe TP303 FILT CV at hole just above U350 and adjust FILT CTF knob to read approximately 5.75V.
4. Probe U433-7 VOICE 1 FILT FREQ SMR by clipping to the right end of R4145.
5. Note reading (e.g., .063V), then turn FILT ENV AMT to 10. Trim R495 for same reading as with FILT ENV AMT knob set to 0.
6. Trim Voices 2 - 5 in the same way, referring to Table 4-3.

Table 4-3
FILTER ENVELOPE AMOUNT VCA BALANCE

VOICE	OTA	PROBE	TRIMMER
1	U433-7	R4145	R495
2	U434-14	R4146	R497
3	U434-1	R4149	R499
4	U434-7	R4154	R4101
5	U434-8	R4157	R4103

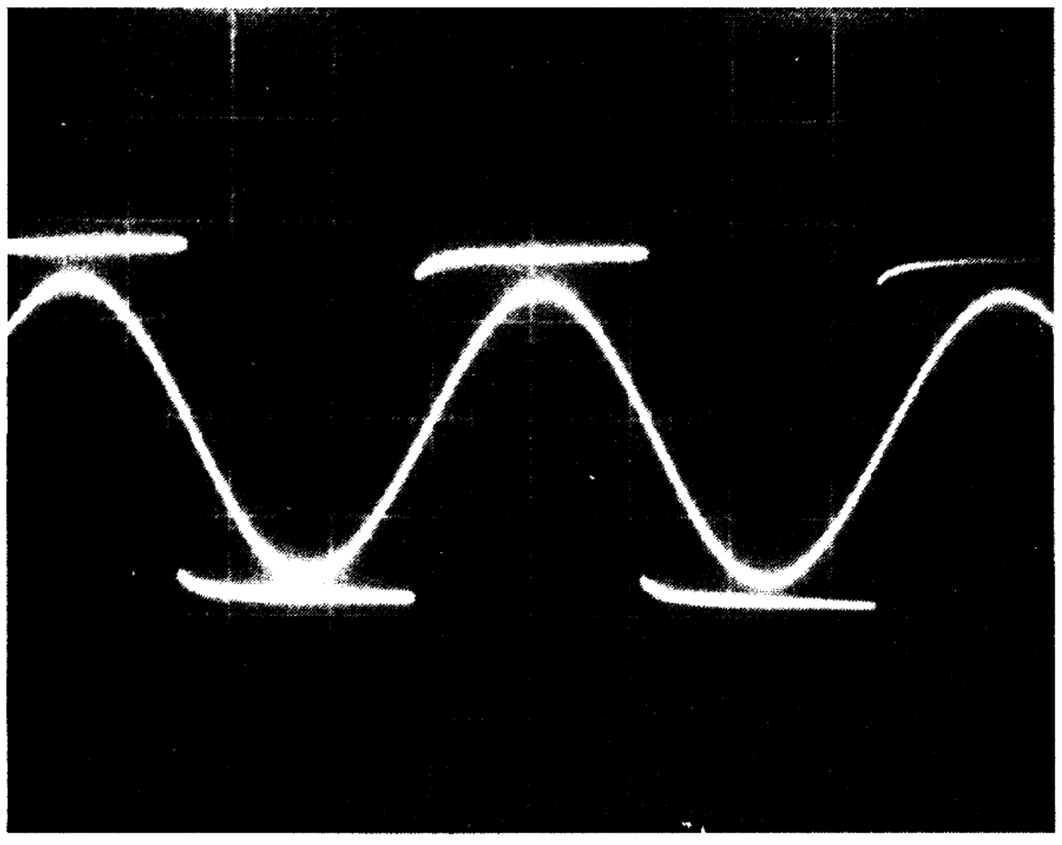
4-20 FILTER TUNING

NOTE: If Rev 3.0 Software level is V.8.1, (original) and VCO SCALE TRIM has been performed, switch power off then back on to reset the A-440 port (otherwise the reference will be left tuned to "C"). If V.8.2 is installed, power-reset will not be necessary because the tuning port is automatically reset when exiting SCALE TRIM routine.

A scope is required for this trim.

Note that there is no computer-correction of filter tuning as there is for the oscillators, so the filters will never track as well as the oscillators. There is also no temperature compensation, so the filters will always drift a certain amount. For this reason, filter tuning can degrade as soon as five minutes after tuning. The filters are gain-matched, with the set code written on PCB 4 just above U469 (e.g. 3.60 - 3.64). Include this set code when ordering replacement filters.

1. Switch PRESET off and set controls according to Figure 4-5.
2. Switch UNISON on.
3. Probe TP303 FILT CV at hole just above U350 and adjust FILT CTF knob to read as close to 2.000V as the quantized voltage steps will allow.
4. Switch A-440 on.
5. Sync scope from TP401, A-440, located above and to the left of U464. It may be easier to clip to the left end of R4498.
6. Probe U474-7 FILT output buffer by clipping on to left end of R4500.
7. Alternately play A3 and A4 (highest A) while tuning R4501 INIT FREQ (OFFSET) and R4133 FILT SCALE for 440- and 880-Hz. The two trimmers interact, so repeat until no improvement is possible. See Waveform 4-0.
8. Trim Voices 2 - 5 in the same way, referring to Table 4-4.



V = .1V/div
H = 5 ms/div

Waveform 4-0
FILTER TUNING

Table 4-4
FILTER TUNING TRIMMERS

VOICE	FILT BUFFER	PROBE	INIT FREQ	SCALE
1	U474-1	R4500-RIGHT END	R4501	R4133
2	U475-1	R4506-LEFT END	R4504	R4134
3	U475-7	R4508-RIGHT END	R4509	R4135
4	U476-1	R4514-LEFT END	R4512	R4136
5	U476-7	R4516-RIGHT END	R4517	R4137

4-21 FINAL VCA BAL

1. Switch PRESET off and set controls according to Figure 4-8.
2. Turn MIX OSC A to 0.
3. Switch FILT KBD off.
4. Switch UNISON on.
5. Tie any key on by clipping J-wire to bus bar.
6. Referring to Table 4-5, turn down Voice 2 - 5 volumes with trimmers listed.
7. Check that R4529 is set for maximum Voice 1 volume.
8. Probe U480-5 at left end of R4565-569.
9. Trim R4520 for .000-V reading.
10. Turn Voice 1 volume all the way down.
11. Turn Voice 2 Volume up fully, and trim in the same way.
12. Repeat for Voices 3 - 5.
13. Untie key.

Table 4-5
FINAL VCA BAL

VOICE	VOLUME	FINAL VCA BAL
1	R4529	R4520
2	R4528	R4521
3	R4527	R4522
4	R4526	R4523
5	R4525	R4524

4-22 VOICE VOLUME

1. Switch PRESET off and set controls according to Figure 4-1 or factory program 1-8.
2. Adjust OSC A FREQ to 5.
3. With scope, probe U480-7 at right end of R4564.
4. Check that all Voice Volume trimmers are set for maximum volume (see Table 4-5).
5. Play polyphonically and measure each voice level on scope. (To identify the voices, touch the OSC As.).
6. Turn down louder voices to volume of the softest voice.

SECTION 5
PARTS

5-0 CHASSIS

NOTE. FOR ITEM DESCRIPTIONS
SEE PARAGRAPH 5-6,
BILL OF MATERIALS

DESIGNATOR	ITEM NO.
F1	E-051
J1/2	J-001
J3	J-014
J4-10	J-001
J11	J-029/P-028
J12	J-043/P-022
J13	J-007 (SEE SA1)
J14	J-044/P-022
P1	E-037
R1/2	R-207
S1	S-025
S2	S-032
S3	S-038
SA1	S-027
T1	E-048
W1	E-080
W2	E-078

5-1 PCB 1

C101	C-045
D101-14	D-005
DS101-14	SEE S101-14
R101-13	R-221
S101	S-028
S102-12	S-029
S113	S-028
S114	S-029

5-2 PCB 2

C201-04	C-045
C205	C-031
D201-23	D-005
DS201-22	SEE S201-22
DS224	L-005
J201	J-007
P201	P-025, P-032
P202	P-040
Q201	T-002
QA201	T-011
R201/02	R-221
R203	R-008
R204/05	R-221
R206	R-008
R207/08	R-221
R209	R-008
R210/11	R-221
R212	R-010
R213-17	R-221
R218-20	R-010
RA201	R-300
RA202	R-301
S201-20	S-028
S221	S-029
S222	S-030
S223	S-031
U201-03	I-211
U204/05	I-227
U206	I-235
U207/08	I-227
U209/10	I-216
U211	I-228
U212	I-218
W201	E-071

5-3 PCB 3

BT301	E-040
C301	C-045
C302	C-031
C303	C-021
C304-15	C-045
C316	C-014
C317	C-031
C318-20	C-045
C321	C-036
C322/23	C-045
C324	C-040
C325/26	C-045
C327-48	C-012
C349/50	C-045
C351	C-046
C352	C-045
C353/54	C-036
C355/56	C-021
C357	C-045
C358	C-047
C359	C-012
C360	C-021
C361	C-014
C362-64	C-012
C365-69	C-045
C370	C-031
C371	C-045
C372	C-012
C373/74	C-045
C375	C-012
C376	C-041
C377-81	C-045
C382	C-041
C383	C-045
C384/85	C-012
C386	C-045
D301-3	D-005
D304	D-001
D305-19	D-005
J301	J-031, J-042, P-031
J302	J-042
P301	P-027
P302	P-029
P303	P-030
P304	P-013
Q301-08	T-003
Q309	T-008

R301	R-025
R302	R-014
R303	R-022
R304	R-010
R305/06	R-011
R307	R-025
R308	R-011
R309	R-010
R310	R-004
R311-13	R-025
R314	R-011
R315	R-025
R316	R-010
R317	R-011
R318	R-025
R319	R-047
R320	R-062
R321	R-064
R322	R-054
R323	R-040
R324	R-025
R325	R-010
R326	R-031
R327	R-022
R328	R-054
R329	R-110
R330	R-162
R331	R-008
R332	R-067
R333	R-212
R334	R-211
R335	R-163
R336	R-144
R337	R-107
R338	R-217
R339	R-218
R340	R-107
R341	R-108
R342/43	R-115
R344	R-144
R345	R-068
R346	R-045
R347-49	R-025
R350	R-167
R351	R-025
R352	R-110
R353	R-012
R354/55	R-110N
R356	R-165
R357	R-110N
R358-60	R-110A
R361/62	R-045
R363-5	R-110B
R366	R-142
R367	R-014

R368/69	R-162
R370	R-014
R371	R-142
R372	R-110N
R373	R-025
R374	R-110
R375	R-008
R376	R-116
R377	R-121
R378	R-110
R379	R-110A
R380/81	R-012
R382/3	R-110B
R384	R-008
R385	R-217
R386	R-218
R387	R-110 A
R388/89	R-008
R390	R-029
R391	R-113
R392	R-161
R393	R-025
R394	R-066
R395	R-018
R396	R-006
R397/98	R-014
R399	R-119
R3100	R-110
R3101	R-025
R3102	R-110
R3103/104	R-128
R3105	R-122
R3106	R-011
R3107	R-113
R3108	R-142
R3109	R-063
R3110	R-012
R3111	R-010
R3112	R-028
R3113	R-012
R3114/115	R-036
R3116	R-038
R3117/118	R-029
R3119	R-015
R3120	R-004
R3121/122	R-011
R3123/124	R-025
R3125	R-035
R3126	R-016
R3127/8	R-012
R3129	R-218
R3130	R-015
R3131	R-065
R3132	R-026
R3133	R-065
R3134	R-006
R3135	R-123
R3136	R-159
R3137	R-139
R3138	R-116
R3139	R-006
R3140	R-004
R3141/142	R-217
R3143	R-004
R3144	R-026
R3145	R-064
R3146	R-012
R3147/148	R-025
R3149/150	R-029
R3151	R-030
R3152	R-004
R3153	R-011

U301-8		I-226
U309		I-230
U310		I-101
U311		I-025
U312	Z-984 (SET)	Z-985 0.V.8.2
U313		Z-986 1.V.8.2
U314		Z-987 2.V.8.2
U315		I-414
U316/17		I-033
U318/19		I-117
U320		I-101
U321		I-102
U322		I-109
U323/24		I-216
U325		I-008
U326		I-503
U327/28		I-237
U329		I-229
U330		I-205
U331		I-209
U332-40		I-228
U341/42		I-205
U343-45		I-209
U346		I-502
U347		I-323
U348		I-305
U349-54		I-312
U355-57		I-211
U358-64		I-312
U365		I-302
U366-68		I-313
U369-71		I-206
U372		I-404
U373		I-312

U374	I-313
U375	I-315
U376	I-321
U377	I-206
U378	I-322
U379	I-233
U380	I-312
U381	I-322
W301	E-079

5-4 PCB 4

C401-02	C-045
C403-09	C-040
C410	C-045
C411-18	C-040
C419/20	C-045
C421/22	C-036
C423	C-031
C424	C-043
C425	C-012
C426	C-014
C427	C-043
C428	C-012
C429	C-014
C430	C-043
C431	C-012
C432	C-014
C433	C-043
C434	C-012
C435	C-014
C436	C-043
C437	C-012
C438	C-014
C439/40	C-045
C441	C-043
C442	C-014
C443	C-043
C444	C-014
C445	C-043
C446	C-045
C447	C-014
C448	C-043
C449	C-014
C450	C-043
C451	C-045
C452	C-014
C453-57	C-045
C458	C-045
C459-63	C-045
C464-66	C-008
C467	C-045
C468	C-008
C469	C-045
C470	C-008
C471-80	C-045
C481	C-039
C482	C-045
C483	C-039
C484	C-045
C485	C-039
C486	C-045
C487	C-039
C488	C-045
C489	C-039
C490	C-045
C491-100	C-012
C4101-104	C-045
C4105	C-021
C4106-110	C-005
C4111-118	C-045
C4119	C-039
C4120	C-045
C4121	C-039
C4122	C-045
C4123	C-039
C4124	C-045
C4125	C-039
C4126	C-045
C4127	C-039
C4128	C-045
C4129-138	C-012
C4139-144	C-045
C4145-149	C-044
C4150-159	C-038
C4160-163	C-045
C4164-168	C-021
C4169-178	C-038
C4179-183	C-045
C4184	C-018
C4185-188	C-045
C4189	C-042
D401-18	D-005
P401	P-013
P402	P-044
Q401-11	T-003
R402-04	R-168
R405-06	R-141
R407-09	R-169
R410-15	R-145
R418/19	R-145
R423-25	R-145

R426	R-141
R427-29	R-169
R430-32	R-168
R433	R-141
R439-43	R-145
R444	R-028
R445	R-040
R446	R-057
R447	R-040
R448/49	R-141
R450	R-147
R451	R-149
R452	R-147
R453	R-171
R454	R-028
R455	R-040
R456	R-057
R457	R-040
R458/59	R-041
R460	R-147
R461	R-149
R462	R-147
R463	R-171
R464	R-028
R465	R-040
R466	R-057
R467	R-040
R468/69	R-141
R470	R-147
R471	R-149
R472	R-147
R473	R-171
R474	R-028
R475	R-040
R476	R-057
R477	R-040
R478/79	R-141
R480	R-147
R481	R-149
R482	R-147
R483	R-171
R484	R-028
R485	R-040
R486	R-057
R487	R-040
R488/89	R-141
R490	R-147
R491	R-149
R492	R-147
R493	R-171
R494-103	R-217
R4104	R-030
R4105/06	R-004
R4107	R-140
R4108/09	R-016
R4110	R-140
R4111/12	R-004
R4113/14	R-030
R4115/116	R-004
R4117	R-140
R4118/119	R-016
R4120	R-140
R4121/122	R-004
R4123/124	R-030
R4125/126	R-004
R4127	R-140
R4128	R-016
R4129	R-012
R4130	R-011
R4131	R-026
R4132	R-012
R4133-137	R-222
R4138-142	R-217
R4143/144	R-110
R4145/146	R-151
R4147/148	R-110
R4149	R-151
R4150-153	R-110
R4154	R-151
R4155/156	R-110
R4157	R-151
R4158	R-029
R4159	R-025
R4160	R-110
R4161/162	R-167
R4163-166	R-110
R4167	R-167
R4168	R-012
R4169	R-030
R4170/171	R-167
R4172-176	R-113
R4177-181	R-114
R4182	R-008
R4183	R-029
R4184	R-146
R4185	R-142
R4186	R-211
R4187	R-012
R4188	R-146
R4189	R-142
R4190	R-211
R4191	R-012
R4192	R-146
R4193	R-142
R4194	R-211
R4195	R-012
R4196	R-146
R4197	R-142

R4198	R-211
R4199	R-012
R4200	R-146
R4201	R-142
R4202	R-012
R4203	R-211
R4204	R-170
R4205/206	R-110
R4207	R-006
R4208	R-139
R4209	R-116
R4210	R-006
R4211	R-170
R4212/213	R-110
R4214	R-006
R4215	R-139
R4216	R-116
R4217	R-006
R4218	R-170
R4219/220	R-110
R4221	R-006
R4222	R-139
R4223	R-116
R4224	R-006
R4225	R-170
R4226/227	R-110
R4228	R-006
R4229	R-139
R4230	R-116
R4231	R-006
R4232	R-170
R4233/234	R-110
R4235	R-006
R4236	R-139
R4237	R-116
R4238	R-006
R4239/240	R-026
R4241-245	R-041
R4246/247	R-026
R4248	R-041
R4249-251	R-026
R4252/253	R-029
R4254/255	R-025
R4256/257	R-029
R4258-261	R-025
R4262/263	R-029
R4264	R-026
R4265/266	R-041
R4267	R-026
R4268	R-041
R4269/270	R-029
R4271-274	R-025
R4275/276	R-029
R4277	R-026
R4278	R-041
R4279	R-108
R4280-289	R-041
R4290	R-107
R4291	R-012
R4292	R-146
R4293	R-142
R4294	R-211
R4295	R-012
R4296	R-018
R4297	R-012
R4298	R-146
R4299	R-142
R4300	R-211
R4301	R-012
R4302	R-018
R4303	R-012
R4304	R-146
R4305	R-142
R4306	R-211
R4307	R-012
R4308	R-018
R4309	R-012
R4310	R-146
R4311	R-142
R4312	R-211
R4313	R-012
R4314	R-018
R4315	R-012
R4316	R-146
R4317	R-142
R4318	R-211
R4319	R-012
R4320	R-018
R4321/322	R-110
R4323	R-006
R4324	R-170
R4325	R-139
R4326	R-116
R4327	R-006
R4328/329	R-110
R4330	R-006
R4331	R-170
R4332	R-139
R4333	R-116
R4334	R-006
R4335/336	R-110
R4337	R-006
R4338	R-170
R4339	R-139
R4340	R-116
R4341	R-006
R4342/343	R-110
R4344	R-006
R4345	R-170
R4346	R-139
R4347	R-116

R4348	R-006
R4349/350	R-110
R4351	R-006
R4352	R-170
R4353	R-139
R4354	R-116
R4355	R-006
R4356	R-008
R4357-361	R-115
R4362	R-025
R4363	R-004
R4364	R-041
R4365	R-004
R4366	R-026
R4367	R-025
R4368/369	R-036
R4370-372	R-004
R4373	R-041
R4374	R-004
R4375	R-026
R4376	R-025
R4377/378	R-036
R4379-381	R-004
R4382	R-041
R4383	R-004
R4384	R-026
R4385	R-025
R4386/387	R-036
R4388-390	R-004
R4391	R-041
R4392	R-004
R4393	R-026
R4394	R-025
R4395/396	R-036
R4397-399	R-004
R4400	R-041
R4401	R-004
R4402	R-026
R4403	R-025
R4404/405	R-036
R4406/407	R-004
R4408	R-058
R4409	R-024
R4410/411	R-025
R4412	R-058
R4413	R-024
R4414	R-026
R4415	R-031
R4416	R-056
R4417	R-058
R4418	R-024
R4419/420	R-025
R4421	R-058
R4422	R-024
R4423	R-026
R4424	R-031
R4425	R-056
R4426	R-058
R4427	R-024
R4428/429	R-025
R4430	R-058
R4431	R-024
R4432	R-026
R4433	R-031
R4434	R-056
R4435	R-058
R4436	R-024
R4437/438	R-025
R4439	R-058
R4440	R-024
R4441	R-026
R4442	R-031
R4443	R-056
R4444	R-058
R4445	R-024
R4446/447	R-025
R4448	R-058
R4449	R-024
R4450	R-026
R4451	R-031
R4452	R-056
R4453	R-024
R4454	R-058
R4455/456	R-025
R4457	R-009
R4458	R-152
R4459	R-139
R4460	R-021
R4461	R-024
R4462	R-058
R4463/464	R-025
R4465	R-009
R4466	R-152
R4467	R-139
R4468	R-021
R4469	R-024
R4470	R-058
R4471/472	R-025
R4473	R-009
R4474	R-152
R4475	R-139
R4476	R-021
R4477	R-024
R4478	R-058
R4479/480	R-025
R4481	R-009
R4482	R-152
R4483	R-139
R4484	R-021
R4485	R-024
R4486	R-058

R4487/488	R-025
R4489	R-009
R4490	R-152
R4491	R-139
R4492	R-021
R4493-497	R-036
R4498	R-012
R4499	R-025
R4500	R-058
R4501	R-212
R4502/503	R-130
R4504	R-212
R4505	R-025
R4506	R-058
R4507	R-025
R4508	R-058
R4509	R-212
R4510/511	R-130
R4512	R-212
R4513	R-025
R4514	R-058
R4515	R-025
R4516	R-058
R4517	R-212
R4518	R-130
R4519	R-015
R4520-524	R-217
R4525-529	R-225
R4530-534	R-036
R4535	R-025
R4536-540	R-026
R4541/542	R-011
R4543	R-025
R4544	R-008
R4545	R-042
R4546	R-021
R4547/548	R-015
R4549	R-021
R4550/551	R-015
R4552	R-021
R4553/554	R-015
R4555	R-021
R4556/557	R-015
R4558	R-021
R4559/560	R-015
R4561	R-021
R4562	R-015
R4563/564	R-014
R4565-569	R-017

U401-04	I-312
U405/06	I-211
U407-10	I-312
U411	I-411
U412-21	I-319
U422-26	I-322A
U427	I-315
U428-30	I-233B
U431-34	I-313
U435	I-301
U436-38	I-206
U439/40	I-211
U441-45	I-312
U446-50	I-206
U451-53	I-312
U454-58	I-321
U459-63	I-206
U464-68	I-322B
U469-73	I-320
U474-76	I-312
U477	I-321
U478-79	I-322C
U480	I-312
U481	I-317

W401	E-079
W402	E-079

5-5 PCB 5

C501	C-036
C502	C-021
C503	C-028
C504	C-025
C505-08	C-021
C509	C-036
C510	C-028

D501-04	D-004
D505	D-001
D506	D-004

R501	R-219
R502	R-158
R503	R-125
R504	R-008
R505	R-156
R506	R-043
R507	R-157
R508	R-219

U501	I-420
U502	I-410
U503	I-411
U504	I-409
U505	I-412

5-6 BILL OF MATERIALS (TOTAL ITEMS)

LINE	ITEM	DESCRIPTION	QTY
000	C-005	200P 50V DISC CAP	5
002	C-008	.001 50V MYLAR 10% CAP	5
004	C-012	.01UF MYLAR 50V	54
006	C-014	.02 50V MYLAR	12
007	C-018	.22 35V TANTALUM	1
008	C-021	2.2 TANTALUM 25V 20% CAP	16
010	C-025	2200 25V ELECTROLYTIC CAP	1
012	C-028	6300 25V CAP	2
014	C-031	10 10V TANTALUM CAP	5
016	C-036	10U 25V TANT	7
018	C-038	150PF POLY 5%	20
020	C-039	1000PF, POLY	10
022	C-040	10,000PF(.01) POLY 50V 5%	16
024	C-041	.1UF MYLAR 50V 5%	2
026	C-042	2.2UF NON-POLAR 25V	1
028	C-043	.039UF MYLAR 5% 50V	10
030	C-044	10UF TANT 3V	5
032	C-045	.1UF 50V DECOUPLER	116
034	C-046	.0056 MYLAR 100V	1
036	C-047	120 PF 10% DISC (WAS 75PF	1
038			
040	D-001	1N4002 100V 1 AMP DIODE	2
042	D-004	MR501(1N5401) 100V 3AMP	5
044	D-005	1N914	73
046			
048	E-001	18 AWG RED	2
050	E-002	18 AWG BLUE	4
052	E-003	BLACK WIRE	5
054	E-017	SQUARE FUSE HOLDER BLACK	1
056	E-018	SQUARE FUSE HOLDER CAP RD	1
058	E-037	PWRCORD BELDEN17238 3C 8'	1
060	E-040	2.9V BATTERY LITHIUM	1
062	E-044	AWG 22 ORANGE--BELDN 8524	4
064	E-045	BLACK COAX 8216-BELDEN	3
066	E-048	CT TRANSFORMER 5V3	1
068	E-051	3\4 AMP SLO-BLO FUSE	1
070	E-053	22 AWG STRANDED YELLOW	2
072	E-054	22 AWG STRANDED BLACK	2
074	E-055	22 AWG STRANDED GREY	2
076	E-056	22 AWG STRANDED WHITE	2
078	E-057	22 AWG STRANDED BROWN	2
080	E-058	22 AWG STRANDED VIOLET	2
082	E-059	22 AWG STRANDED RED	4
084	E-060	22 AWG STRANDED TAN	2
086	E-061	22 AWG STRANDED LGHT BLUE	4
088	E-062	22 AWG STRANDED GREEN	4
090	E-063	18 AWG WHITE	2
092	E-064	18 AWG ORANGE	1
094	E-065	18 AWG YELLOW	2

096	E-066	18 AWG WHITE W\ORANGE STR	1
098	E-071	40 PIN RIBBON CABLE	1
100	E-078	RIB CBL 60COND MLX 2.75"	1
102	E-079	BUS BAR	3
104	E-080	RIBBON CABLE, 16-PIN	1
106			
108	I-008	7474 IC TTL DUAL FLIPFLT	1
110	I-025	Z-80 CPU	1
112	I-027	2708 1024X8 EPROM	3
114	I-033	2114 1024X4 STATIC RAM	2
116	I-101	74LS00 IC LSTTL QUAD NAND	2
118	I-102	74LS02 IC LSTTL QUAD NOR	1
120	I-109	74LS74 LSTTL DUALFLIPFLOP	1
122	I-117	74LS138 3-8 DECODER	2
124	I-205	4013 CMOS DUAL FLIPFLOP	3
126	I-206	4016 CMOS QD ANALOG SWTCH	17
128	I-209	4049 CMOS HEX INVTR\DRIVR	4
130	I-211	4051 CMOS 8-IN AN MULTPLX	10
132	I-216	4503 CMOS HEX 3STATE BUFF	4
134	I-218	4514 CMOS 4-16 DE-MULTPLX	1
136	I-226	6508 CMOS 1K X1 L PWR RAM	8
138	I-227	4042 QUAD LATCH	4
140	I-228	4174 HEX LATCH	10
142	I-229	4556 DUAL 2-4 DEMUX	1
144	I-230	74C02 QUAD NOR	1
146	I-233	14066B QUAD ANALOG SWITCH	1
148	I-235	MC1413(2003)	1
150	I-237	14504 HEX LEVEL SHIFTER	2
152	I-301	311 PRECISION COMPARATOR	1
154	I-302	339 QUAD COMPARATOR	1
156	I-305	LM741CN OP AMP	1
158	I-312	TL082 DUAL BIFET OP AMP	30
160	I-313	LM348 QUAD-741 OP AMP	8
162	I-315	MM5837N NOISE SOURCE	2
164	I-317	NE5534, SIGNETICS	1
166	I-319	3310 ENV GEN	10
168	I-320	3320 VCF	5
170	I-321	3340 VCO	11
172	I-322	3280 DUAL OP TRNSCND AMP	18
174	I-323	LF356 FET OP AMP	1
176	I-404	78M05CT	1
178	I-409	MA78M12UC +12 1\2 AMP REG	1
180	I-410	MA7805VC +5V1AMP(LM340T-5	1
182	I-411	LM7905/79M05 -5V 1A REG	2
184	I-412	LM317T +15V 1AMP REG	1
186	I-414	8253 TIMER	1
188	I-420	LM337T NEG ADJ REG 1-27V	1
190	I-502	16 BIT DAC 71-CSB-I	1
192	I-503	XO-12C, 5-MHZ, DALE	1
194			
196	J-001	1/4" PHONE, SHORTING	9
198	J-007	16-PIN DIP SOCKET	48
200	J-014	SWITCHCRAFT 113 MONOJACK	1
202	J-016	40 PIN DIP SOCKET	1

204	J-017	24 PIN DIP SOCKET	5
206	J-028	3 PIN JACK	1
208	J-029	20 PIN JACK	1
210	J-031	10 PIN MOLEX JACK GOLD	1
212	J-041	18-PIN DIP SOCKET(BURNDY	7
214	J-042	6-PIN MOLEX JACK GOLD	2
215	J-043	7-PIN MOLEX HOUSING	1
216	J-044	2-PIN MOLEX HOUSNG	1
218			
220	L-005	DIS 6740 DL DIG .56 MAN	1
222			
224	M-002	RED PLEXIGLASS 11\2"X2"	1
226	M-005	PLASTIC TIES	2
228	M-009	LARGE STRAIN RELIEF	1
230	M-016	LARGE RUBBER FEET	4
232	M-020	TERM RING LUGS 12GAUGE#10	1
234	M-025	5\16"BLK FLATHEAD PHILLIP	4
236	M-027	SHEETMETAL SCREWS	36
238	M-031	6-32 LOCKWASHERS EX TOOTH	7
240	M-035	6-32 NUTS SMALL	11
242	M-039	700/SCI LABEL, LONG	1
244	M-054	SYNTHESIZER WOOD BOX	1
246	M-056	SYNTH FRONT COSMETC STRIP	1
248	M-068	STICKER SMALL "PROPHET-5"	1
250	M-069	STICKER SMALL SCI	1
252	M-070	1\2 6-32 SET SCREWS	2
254	M-071	1\4"6-32 PANSLTSCREW MS2P	9
256	M-073	30-1 TENSION CLIP-PW DET	1
258	M-079	KNOB BLCK TOP SPRING CLIP	24
260	M-080	KNOB SILVR TOP SPRNG CLIP	2
262	M-081	THERMALLOY 43-66-2AP	3
264	M-082	CAP HOLDER TH25 MALLORY	2
266	M-085	CLAMP FOR RIB CBLE CFCC-4	1
268	M-088	DBL CBLE CLMP RICHCO UC-2	2
270	M-089	8-32 3\8" PANSLT MS SCREW	4
272	M-090	XLUTS 6-32 LARGE	2
274	M-091	NUTS 8-32 HEX	6
276	M-092	#8 LOCKWSHR INTRNL TOOTH	6
278	M-093	SCREW 1\2" 8-32 PANHD SLT	6
280	M-095	TERMINL RING RED PV18-10R	1
282	M-097	1000 SERIAL # LABELS	1
284	M-107	NYLN SHLDRWSHR - REG #411	3
286	M-111	1 1\4STANDOFF 1\40D 6-32	4
288	M-112	3\4 STANDOFF 1\40D 6-32	2
290	M-117	FOAM RBBR1"W 1\16T W\PSA1	5
292	M-119	6\32X5\8BLK PHLLPS M\S	4
294	M-124	HEATSINK	1
296	M-182	3/8" STARWASHER	10
298	M-140	TIE	2
300	M-150	SHRINK TUBING 3/16"	1
302	M-151	SHRINK TUBING 1/4"	1
304	M-152	POT NUT	26
306	M-154	#8 FIBER WASHERS	4
308	M-155	1/2" STANDOFF SMITH8343	6

310	M-156	3/8" X 6-32 PHLP CNTRSNK	25
312	M-157	4-40 X 1/4" BLCK PNHDSLT	3
314	M-158	8-32 X 1/2" BLK PANHDSLT	4
316	M-159	3/16" WIDE FOAM TAPE	1
318	M-160	MEDIUM "PROPHET-5" STCKR	1
320	M-161	8-32 X 3/4" PNHDSLT	2
322	M-200	SYNTH WHEEL, 5V3	2
324	M-201	CONTROL PANEL,5V3	1
326	M-202	WHEEL BOX,5V3	1
328	M-203	BOTTOM PANEL,5V3	1
330	M-204	WHEEL BRACKET,5V3	2
332	M-205	KEYBOARD BKT,5V3	1
334	M-206	HEATSINK,BACK PNL	1
336	M-211	PCB1,5V3	1
338	M-212	PCB2,5V3	1
340	M-213	PCB3,5V3	1
342	M-214	PCB4,5V3	1
344	M-215	PCB5,5V3	1
346			
348	P-013	60 PIN HEADER AP	2
349	P-022	PINS GOLD	8
350	P-025	10PIN PLUG GOLD	1
352	P-027	7-PIN POLAR. RT-ANGLE	1
353	P-028	GOLD SOCKETS CONTACT	23
354	P-029	20 PIN PLUG GOLD	1
356	P-030	3 PIN PLUG GOLD	1
358	P-031	POLARIZING PINS	2
360	P-032	5 PIN PLUG	1
362	P-040	6 PIN MOLEX ST	2
364	P-044	2-PIN MOLEX GOLD PLUG	1
366			
368	Q-001	PACKING TAPE	1
370	Q-005	1" GLASS TAPE	1
372	Q-009	28X50X.002 BAGS M 1000	1
374	Q-014	WARRANTY CARD	1
376	Q-036	1000.3 OP MAN (CM1000C)	1
378	Q-017	1000 PACKING BOX	1
380			
382	R-004	330 OHM 1\4W 5%	35
384	R-006	470 OHM 1\4W 5% RESISTOR	23
386	R-008	1K 1\4W 5% RESISTOR	12
388	R-009	1.5K 1\4W 5% RESISTOR	5
390	R-010	2K 1\4W 5% RESISTOR	9
392	R-011	4.7K 1/4W 5%	12
394	R-012	10K 1\4W 5% RESISTOR	27
396	R-014	15K 1\4W 5% CARBON FILM	7
398	R-015	20K 1\4W 5% RESISTOR	14
400	R-016	30K 1\4W 5% RESISTOR	6
402	R-017	39K 1\4W 5% RESISTOR	5
404	R-018	47K 1\4W 5% RESISTOR	6
406	R-021	68K 1\4W 5% RESISTOR	11
408	R-022	75K 1\4W 5% RESISTOR	2
410	R-024	91K 1\4W 5% RESISTOR	15
412	R-025	100K 1\4W 5% RESISTOR	63

414	R-026	200K 1\4W 5% RESISTOR	28
416	R-028	470K 1\4W 5% RESISTOR	6
418	R-029	1M 1\4W 5% RESISTOR	17
420	R-030	2.2M 1\4W 5% RESISTOR	7
422	R-031	3K 5% RESISTOR	6
424	R-035	2.7K RESISTOR	1
426	R-036	3.3K RESISTOR	22
428	R-038	8.2K RESISTOR	1
430	R-040	22K, 5%	11
432	R-041	150K RESISTOR	25
434	R-042	560 OHM RESISTOR	1
436	R-043	47 OHM 5% RESISTOR	1
438	R-045	10M 5% RESISTOR	3
440	R-047	10 OHM 5% 1\4W RESISTOR	1
444	R-054	33K, 5%	2
446	R-056	51K,5%	5
447	R-057	120K,5%	5
448	R-058	240K,5%	20
452	R-062	5.6K, 5%	1
454	R-063	910, 5%	1
456	R-064	5.1K, 5%	2
458	R-065	160K, 5%	2
460	R-066	300K, 5%	1
462	R-067	3.9K, 5%	1
464	R-068	100, 5%	1
466	R-107	4.99K 1% RESISTOR	3
468	R-108	10K 1% RESISTOR	2
470	R-110	100K 1% 1/4W	55
472	R-113	30.1K 1% RESISTOR	7
473	R-114	54.9K 1% RESISTOR	5
474	R-115	301K RESISTOR 1%	7
475	R-116	2.21M 1% 1\4W RESISTOR	12
476	R-119	13.3K 1% RESISTOR	1
478	R-121	1M, 1%	1
479	R-122	200K 1% RESISTOR	1
480	R-123	487K 1% RESISTOR	1
482	R-125	121, 1% RN55D1210F	1
484	R-128	182K 1% RESISTOR	2
486	R-130	249K 1% RESISTOR	5
487	R-139	1.82K, 1%	16
488	R-140	3.32K, 1%	5
490	R-141	4.75K, 1%	14
492	R-142	5.62K, 1%	13
494	R-144	20.0K, 1%	2
495	R-145	24.3K, 1%	16
496	R-146	26.7K, 1%	10
498	R-147	47.5K, 1%	10
502	R-149	121K, 1%	5
504	R-151	162K,1%	5
506	R-152	187K, 1%	5
510	R-156	243, 1%	1
512	R-157	2.55K, 1%	1
513	R-158	1.24K, 1%	1
516	R-159	110K, 1%	1

518	R-161	24.9K, 1%	1
520	R-162	332, 1%	3
522	R-163	18.2K, 1%	1
524	R-165	261K, 1%	1
528	R-167	52.3K, 1%	6
530	R-168	806, 1%	6
532	R-169	13.0K, 1%	6
534	R-170	357K, 1%	10
536	R-171	475K, 1%	5
544	R-207	JA1G0405104UA 100K POT	2
546	R-211	5K TRIMMER 1TURN TOP ADJ	11
548	R-212	100K TRIMMER 1TURN TP ADJ	6
550	R-217	100K TRIM,1TURN TOP PIHER	25
552	R-218	10K TRIM, 1TURN TOP PIHER	2
554	R-219	200 OHM TOP ADJ TRIMMER	2
556	R-221	SPECIAL 10K LIN POT	26
558	R-222	50K CERMET BOUR3386P1503	5
564	R-225	25K 1-TURN TOP ADJ PIHER	5
572	R-300	39-OHM X 8 NTWK, BOURNS	1
574	R-301	22K-OHM X 15 NTWK, BOURNS	1
576			
578	S-025	AC POWER SWITCH LIGHT RED	1
580	S-027	5-OCT KYBD 10-0-0218-1	1
582	S-031	SWITCH GREY SR	1
584	S-032	115/230 SLIDE SW 46206LFR	1
586	S-034	FOOTSWITCH	1
588	S-038	REC ENABLE\DIS SLIDE SW	1
590	S-028	BLACK LED SWITCH SRL	22
592	S-029	GREY LED SWITCH SRL	13
594	S-030	ORANGE LED SWITCH SRL	1
598			
600	T-002	2N3904 PNP TRANSISTOR	1
602	T-003	2N4250 PNP TRANSISTOR	19
604	T-008	AD820 MATCHED PNP PAIR	1
606	T-011	3082 RCA	1

SECTION 6
GLOSSARY

This list covers abbreviations appearing on SCI documentation except that integrated circuits are generally shown with the manufacturer's abbreviations. Refer to the device data sheet as required.

A	address bus
A	VCO A
A	Ampere
(a), (A)	analog (for power or common)
AC	alternating current
ACC	accumulator
ACK	acknowledge
A/D	analog/digital (hybrid)
ADC	analog-to-digital converter
ADJ	adjust
ADPT	adapter
ADSR	attack/decay/sustain/release (ENV GEN)
AH	address bus, high-voltage
ALU	arithmetic-logic unit
AM	ammeter
AMP	amplifier (FIN VCA)
AMT	amount
APPROX	approximate
ASSY	assembly
ATK	attack
ATT	attenuation, attenuator
AUX	auxiliary
AVG	average
B	VCO B
B	bit number (LSB, MSB)
BAL	balance
BANK	bank
BCD	binary-coded-decimal
BFR	buffer
BLK	black
BLU	blue
BRN	brown
BT	battery (designator)
C	capacitor (designator)
C	control (solid-state switch)
°C	Centigrade
CAL	calibration, calibrator
CASS	cassette
CB	circuit breaker (designator)
CC	control current for OTAs
CCW	counter-clockwise
CHG	charge
CKT	circuit
CLK	clock
CLR	clear
cm	centimeter
CM	current mirror
CMOS	complementary metal-oxide semiconductor
CMP	compensation
CNT	count
CNTR	counter
COAX	coaxial
COMM	common
COMP	computer
CONT	control
CONV	conversion, converter
CPR	comparator
CPU	central processor unit
CR	rectifier module (designator)
CS	chip select
CTF	cutoff
CTR	center
CV	control voltage
CW	clockwise
CY	carry
D	data
D	diode (designator)
(D)	digital (for power or common)
DA	diode array (designator)
DAC	digital-to-analog converter
dB	decibel
DB, DBUS	data bus
DBH	data bus, high-voltage
dc	direct current
DCOD	decoding, decoder
DET	detection, detector
DI	data in
DIP	dual in-line plastic (package)
DIS	disable
DISCHG	discharge
DMUX	demultiplexing, demultiplexer
DO	data out
DN	data, non-volatile
DRVR	driver
DS	indicator (designator)
DSP	display
DVM	digital voltmeter
DX	switch matrix row
DY	switch matrix column
EDIT	edit
EN	enable
ENV	envelope
EOC	end-of-conversion
EOT	end-of-tape
EPROM	erasable-programmable read-only memory
EQ	equalization, equalizer
EXT	external

F	Farad
F	fuse (designator)
F	Farenheit
FDBK	feedback
FET	field-effect transistor
FF	flip-flop
FILT	filter (VCF)
FIN	final
FINE	fine
FOA	(for FACTORY USE ONLY)
FREQ	frequency
FSK	frequency-shift keying
FT	foot
FTSW	footswitch
G, GATE	gate
GEN	generator
GLD	glide
GND	ground
GRN	green
H, HEX	hexadecimal (base 16)
Hz	Hertz
I	inhibit
I	input (solid state switch)
Iabc	amplifier bias current (3280 control)
IC	integrated circuit
IN	input
INIT	initial
INT	interrupt
INV	inversion, inverter
I/O	input/output
IRQ	interrupt request
J	jack (female pins)
JSTK	joystick
K	kilo-
KBD	keyboard
L,	lower
LD	load
LED	light-emitting diode
LFO	low frequency oscillator
LFT	left
LIM	limit, limiter
LIN	linear
LOG	logarithmic
LSB	least significant bit
LSI	large-scale integration
LVL	level
m	mili-
M	mega-
MAX	maximum
MEM	memory
MIN	minimum
MIX	mixer
MOD	modulation
MOS	metal-oxide semiconductor
MSB	most significant bit
MSI	medium-scale integration
MSUM	master summer
MTUN	master tune
MUX	multiplexing, multiplexer
n	nano-
N	non-inverting input
NC	no connection
NC	normally closed contact
NEUT	neutral
NO	normally open contact
NOM	nominal
NORM	normal
NSE	noise
NVM	non-volatile memory
O	output (solid-state switch)
OBS	obsolete
OFST	offset
ORG	orange
OSC	oscillator (VCO)
OTA	operational transconductance amplifier
OUT	output
OV	overflow
p	pico-
P	plug (designator)
P-	polyphonic (modulation)
PBND	pitch bend
PC	program counter (in CPU)
PCB	printed circuit board
PED	pedal
PNK	pink
PNL	panel
POS	positive
POT	potentiometer
PR	pair
PRGM	program
PRGMR	programmer
PROM	programmable read-only memory
PRST	preset
PS	program select
PSB	power supply board
PW	pulse width
PWM	pulse-width modulation
PWR	power
Q	transistor (designator)
QA	transistor array (designator)
QTY	quantity
R	resistor (designator)
RA	resistor array (designator)
RAM	random-access memory
REC	record
REF	reference
REG	regulation, regulator
REL	release
RES	resonance
REV	revision
RGT	right
RIP	ripple clock
ROM	read-only memory
RS	reset
RST	restart
S	switch
S	analog switch signal
SA	switch array (designator)
SAR	successive approximation register
SEC	second

SEL	select
SEQ	sequencer
SER	serial
S/H	sample and hold
SHT	sheet
SIG	signal
S/N	signal-to-noise ratio
S/N	serial number
SPAD	scratchpad (RAM)
SPK	spare parts kit
SPKR	speaker
SRC	source
ST	start
STRB	strobe
SUM	summation, summer
SUS	sustain
SYM	symmetry
SYNC	synchronization, synchronizer
SYNTH	synthesizer
SYS	system
T	transformer (designator)
TB	terminal board (designator)
TC	time constant
THRS	threshold
TP	test point (designator)
TRI	triangle-wave
TRIG	trigger
TRIM	trimming, trimmer
TTL	transistor-transistor logic
TUN	tune
u	micro-
U	integrated circuit (designator)
U,	upper
UART	universal asynchronous receiver-transmitter
UNI	unison
USART	universal synchronous-asynchronous receiver-transmitter
V	Volts
V(A)	V supply, analog circuit
V(D)	V supply, digital circuit
V-C	voltage-to-current converter
VCA	voltage-controlled amplifier (AMP)
VCF	voltage-controlled filter (FILT)
VCO	voltage-controlled oscillator (OSC)
VDAC	DAC output voltage
VIOL	violet
VMUX	POT MUX output voltage
V/OCT	volts-per-octave
VOL	volume
VPED	pedal voltage (or, voltage pedal)
VR	voltage regulator (designator)
VREC	voltage record
W	wiring or cable
W-	wheel (MOD)
WHT	white
XOR	exclusive-OR
Y	crystal
YEL	yellow

SECTION 8

THEORY

8-0 INTRODUCTION

This is the first section of supplementary material appended to the Rev 3.0 Technical Manual which covers the series referred to as Rev 3.1 and 3.2.

The updates and expansion of the microcomputer's memory configuration which became Rev 3.1 are transparent, so, of no interest to the player. But once the Polyphonic Sequencer for the Prophet-10 was designed, we couldn't resist developing one for the Prophet-5. Thus, shortly after Rev 3.1 went into production, we again redesigned the Prophet-5 computer (and a few other circuits) to allow it to interface with the Model 1005 Polyphonic Sequencer and Model 1001 Remote Keyboard/Controller. Therefore if they desire to use these products, owners of Rev 3.0 and 3.1 Prophets will need to have their instruments upgraded to Rev 3.2.

Rev 3.0 started with serial number 1300. Specific tables of 3.1 and 3.2 serial numbers and software versions are in Section 11. If you are in doubt about a Prophet's Rev, just look at the silk-screening on PCB 3. Both revisions 3.0 and 3.2 have the numbers silk-screened at the center top edge of the board. (Note that revision 3.0 is simply called revision 3.) Revision 3.1 has the number screened at the top left corner of the board.

8-1 REVISION 3.1 COMPUTER and POWER SUPPLY

Please refer to SD341 in Section 10. Revision 3.1 incorporates changes to the computer operating system PROM and the Non-Volatile program RAM. For PROM, U312/13 2716 2-K units were put in place of the three 2708 1-K units in Rev 3.0. This allowed the use of a higher-reliability part, elimination of the +12V and -5V power supplies, and created program space for the diagnostic memory test. (The tests are covered in Section 11.)

To use the higher-density 2716s, the CPU address lines to U318 Memory Address Decoder are shifted up to A12-A14. A11 was provided for later updating this board with a 2732 4-K. As shown, it is normally disconnected from the CPU. Instead, the A11 lines to U312-U314 sockets are tied high. (On the 2716, pin 21 is for the Vpp programming pulse.)

The eight 6508 (1K x 1) NV RAM was changed to U383/84, two 4334 or 6514 (1K x 4). These parts have a higher reliability than the parts previously used. To achieve the correct timing, the 3.1 (and 3.2) -NV WRITE signal is generated very differently from the way it is in Rev 3.0. NAND-Gate U382-8 is wired as an inverter. Thus when U311-19 CPU -MREQ goes low, and A15 goes high, U382-11 goes low. U382-6, also an inverter, goes high, raising U320-13. If S3 RECORD is set to ENABLE, U320-12 will also be high, causing U320-11 to go low, enabling the NV RAM -WR inputs.

The Power Distribution area of the schematic shows the spare pins (2 and 3) on P302 created by removing the +12V and -5V lines from PCB 3. The back-panel cable wires to these pins may or may not exist in a specific 3.1 unit. But on all 3.1 units, the regulators and associated components were removed from PCB 5. (See SD541.)

An additional, simple change was made to the CPU which has absolutely no effect on operation. U311-25 -BUSRQ is a CPU output which in REV 3.0 was tied high. In Rev 3.1 this pin is pulled high through R3154 for optional use with factory test instruments.

SD342 shows how TP304 was added to U324-10 ADC BUS DRIVER, pulled low through R3155. Tying this point high starts the memory test routine, as discussed in Section 11.

8-2 REVISION 3.2 COMPUTER and USART

Rev 3.2 was created to interface with the Model 1005 Polyphonic Sequencer and Model 1001 Remote Keyboard/Controller. In order to arrange the interface, the operating system was again expanded and communication circuitry added. Changes were also made to the Common Analog circuitry to accomodate PITCH and MOD CV inputs (see para. 8-3).

See BD051 Rev 3.2 Interconnect Diagram. J17 DIGITAL INTERFACE jack on the back panel is a 4-pin Switchcraft SL-17-4F, SCI #J-053. To mate, use SL-40-4M, SCI #P-053. This jack is cabled along with ANALOG inputs from J16 (see below) through J15, to added connector P305. SD351 shows the DIGITAL CABLE destination, U386 SIGNETICS 2661 Programmable Communications Interface. This USART exchanges data with a compatible transciever over three lines as specified below. System interface programming is discussed in Section 9 (as well as in the current Prophet-5 Operation Manual, CM1000C.1).

WARNING! This is not an RS-232 interface. It uses 5-V TTL levels. RS-232 voltage levels (+/- 12 or +/-15V) will most likely blow the two input gates. Furthermore, most RS-232 interfaces lack the speed required for transparent sequencer-Prophet communications.

Pin 1, GROUND

Pin 2, CLOCK TO SYNTH
This input sees pin 2 of a 74LS08 (U385-3), with a 10K pull-up to +5V. Note that the transmit and receive clocks (TxC, RxC) are tied together. Maximum frequency: 625 kHz. Minimum clock frequency for "transparent" real-time sequencer operation depends on exact operations involved. Slower speeds will generally degrade performance by causing the Prophet to wait too long for the sequencer to complete multi-byte data transfers. 50 kHz is probably as slow as anyone is likely to find useful.

Pin 3, DATA TO SYNTH
This input sees pin 4 of a 74LS08 (U385-6), with a 10K pull-up to +5V. Data format is discussed in Section 9.

Pin 4, DATA FROM SYNTH
This is a MOS output direct from pin 19 of the Signetics 2661 USART. The driver Low output voltage (V_{OL}) is specified at 0.4V max. with a 2.2 mA output current (I_{OL}). The driver High output voltage (V_{OH}) is 2.4V min., specified at -400 uA (I_{OH}).

Digital Cable Specifications
The cabling used depends on the distance desired between units, and upon the noise present in the system environment. Using individual coaxial cables for the two data and clock lines will work best. It is likely you could have trouble-free operation at 20-ft or longer. Three-conducter coax will probably work up to 10 ft. Single wires may be used

for the 2 to 5-foot range. The clock speed influences cable performance, since data transfered at higher speeds encounters more reactance (hence, degradation) in the cable.

USART OPERATION

Normally U386 USART stands unused. But it is initialized to interrupt the CPU when serial data is received. When the CPU is interrupted, it stops whatever it is doing and reads the USART data as if it were reading a memory device. The CPU can also output a byte to the USART. As discussed in the section on programming, this data exchange enables sequencing and remote keyboard control.

In more detail, pin 21 RESET connects to the CPU -RESET through inverter-wired U382-3. When power comes on, RESET clears the USART's internal registers and sets it to Idle. To operate, it must be initialized with the appropriate bytes sent to its control registers.

The USART connects to the Address Bus. A0 and A1 select, while A15 actually programs the reading and writing to or from the USART's receive, transmit, or control registers.

While the Address Bus is used to program the USART, its data lines remain tri-stated until pin 11 -CS goes low. The CPU sends commands and output data to the USART over the Data Bus. The USART sends input data and its own status bytes (as opposed to status bytes sent by the external sequencer) to the CPU.

After resetting and initializing the USART, it is set-up to respond to data input as follows. Through the Low-Voltage Ouput Port Decoder U319, the CPU sets pin 10 -CSOL5 low. On Rev 3.0 this signal cleared the monophonic sequencer interface to GATE 5. On Rev 3.2 this signal clears the Interrupt Flip-Flop U330-2 (see SD352), while GATE 5 is controlled separately. (GATE 5 is now memory-mapped. It is enabled by U318-10, through inverter U343-6 and Flip-Flop U330-13.)

Once the Flip-Flop is reset, U330-2 -INT is high. Notice U385-8, the AND gate (converted to negative logic by DeMorgan) connected to USART pin 14 RxRDY. -INT connects to U385-9. Pin 10 is pulled high by R3153. Thus, with both inputs high, U385-8--which actually connects to the CPU--is high and the CPU runs normally.

The CPU is interrupted either by the USART signalling that it has received a byte, or by a GATE occuring through the monophonic sequencer interface. In the first case, the USART RxRDY pin goes low when the USART has received a serial data byte. Whenever the -INT occurs, the CPU first examines the USART to see if its receiving register is holding data. If not, then the -INT must have arisen from the monophonic sequencer interface.

In this second case, the high SEQ GATE IN (J3) is inverted by U331-4, delayed slightly, and re-inverted by U331-2 to clock the Interrupt Flip-Flop U330-2. Since pin 5 D is tied high, pin 1 Q goes high, and pin 2 -Q goes low, generating the -INT.

8-2 REVISION 3.2 ANALOG and POWER SUPPLY

J16 ANALOG INTERFACE connector is SCI #J-054. To mate, use SL-40-5M, SCI #P-054. The pin specifications are:

WARNING! Since we have no idea what you will be connecting to these inputs, we cannot guarantee this interface will work with any custom device. You are completely responsible for any damage to the Prophet which may result from connecting non-SCI accessories.

Pin 1, GROUND

Pin 3, +22V, unregulated, 50 mA
Pin 5, -22V, unregulated, 50 mA
These two supplies have 5.1-ohm current-limiting resistors (see SD551). But accessories should be fully tested with another power source before connecting to these supplies. WARNING! The Prophet can be damaged if these supplies are tampered with. For best protection of the Prophet, it is best to avoid using these supplies.

Pin 4, PITCH WHEEL CONTROL VOLTAGE INPUT (P-WH CV IN)
This input raises or lowers the pitch of all five voices. The voltage applied should be nominally zero for the instrument to be tuned to A-440. Both positive and negative voltages can be applied. The Prophet disables this input during its TUNE routine to prevent accidental detuning.

Pin 2, MODULATION WHEEL CONTROL VOLTAGE INPUT (M-WH CV IN)
This input ranges 0 - +10V, with maximum modulation being applied at +10V. Do not apply a negative voltage to this input.

Rev 3.2 changes to the Common Analog section are shown on SD354. The MOD Wheel circuitry has gained a Summer U374-8 to add the Mod Wheel CV and an external Mod CV together. VCA U381-12 allows the remote voltage control, and introduces WHEEL BAL trimmer R3168. Trim procedure is in Section 11.

Remote PITCH CV input required switch U377-10 to disable this input during the TUNE routine.

SECTION 9

PROGRAMMING

9-0 INTRODUCTION

This section is the software guide to the system interface distinguishing Rev 3.2 Prophet-5s. The interface was specifically designed to accomodate the Model 1005 Polyphonic Sequencer, Model 1001 Remote Keyboard/Controller, and other accesories. But to encourage experimentation with remote programming of the Prophet we publish this specification for enthusiasts who would design their own sequencer/controller. Many of the popular microcomputers can now be interfaced to the Prophet-5.

All the information you need to use the interface is below. The programs required to transmit keyboard status and to process external keyboard and program commands are contained within the Prophet's own software. This considerably simplifies your sequencer software design into the data exchange of "bit maps" of the keyboard as it is recorded or played. The sequencer never enters into the Prophet's operating system itself, so your experiments can not "hurt" the Prophet by faulty programming. (Although you can of course cause damage with faulty hardware.) The Prophet's operating system is in PROM and remains unaltered, no matter what you do. At worst you will erase the Non Volatile (NV) RAM which stores the "sound" programs. But the programs are easily re-loaded through the standard CASSETTE interface. (The Model 1005 stores and loads programs through this system interface.)

This is a high-speed serial interface, with the clock supplied by the external sequencer or keyboard. We can recommend the SIGNETICS 2651 or 2661 Programmable Communications Interface, which is essentially a microcomputer-oriented USART (Universal Synchronous/Asynchronous Receiver-Transmitter), because it is what the Prophet uses. The 2661 can be clocked to 1 MHz. The Model 1005 clocks the Prophet at 625 kHz. Not all USARTs will operate at the speeds required, so choose carefully. USARTs are probably the easiest to use, but other techniques are possible. A cleverly-programmed microprocessor could drive the interface directly, as could discrete logic.

9-1 Data Format

Both the DATA TO and DATA FROM SYNTH signals use the standard asynchronous serial format; start bit, eight data bits, parity (odd), stop bit. Start bit is low, data is positive, stop is high.

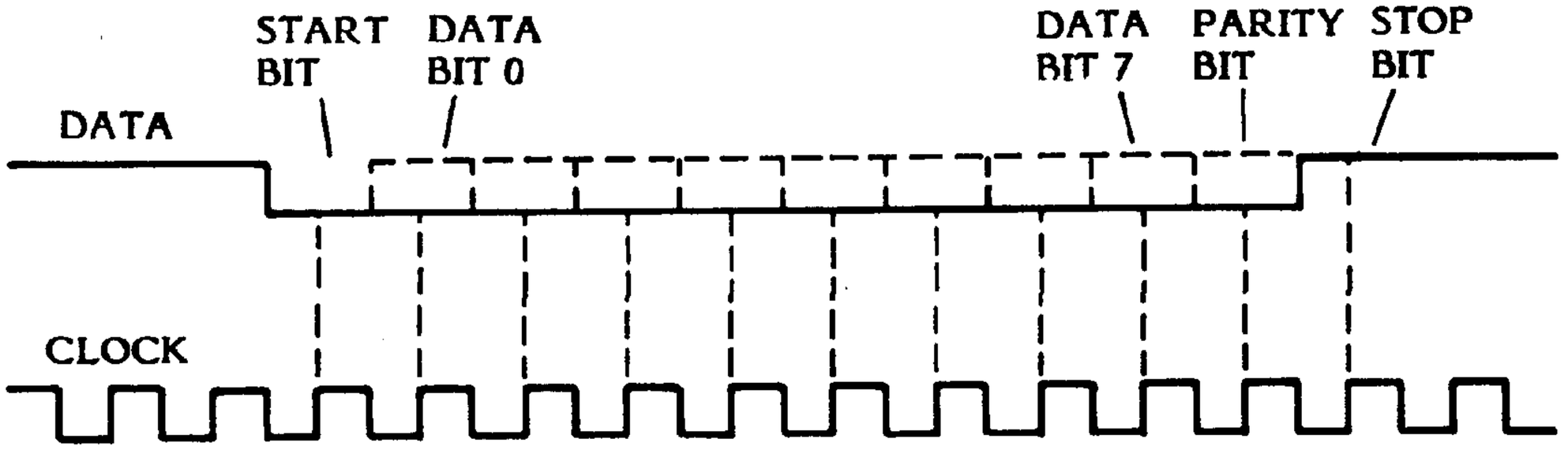


Figure 9-0
DATA FORMAT

At the speed this system normally operates, completely asynchronous operation was not possible. Therefore the external circuitry provides its own normally-high clock. Clock division is not used, so during data transmission a clock pulse must accompany each data bit. As shown, the Prophet receiver samples DATA TO on the rising edge of the clock. The clock should be free running, but the system will work if the clock toggles only during data transmission.

9-2 Error Checking

When it receives data, the Prophet receiver interrupts its CPU which examines a status register in the receiver. The status register indicates if there are any errors. If there is an error, the Prophet transmits code 3F on DATA FROM SYNTH.

There are three possible types of errors: parity, framing, and overrun.

Odd parity works by counting the total number of the data bits and the parity bit (9 total) which are set. If one, three, five, or seven data bits are set (1), parity is already odd, therefore the parity bit is left reset (0). If zero, two, four, six, or eight data bits are set, the parity bit is set to make the total set bit count odd. The Prophet checks DATA TO for parity. The Prophet sends the parity bit with DATA FROM. However, you may choose to ignore parity at your sequencer receiver.

A framing error results when the receiver doesn't find a stop bit at the end of the byte. In a standard asynchronous system this could be caused by a gross difference in transmit and receive clock frequencies. On this system there is a single clock, so a framing error may only result from actual data loss or noise.

An overrun error results when data is being sent too fast for the Prophet receiver to process it (or, by not allowing enough time between bytes). So, this error results from transmit timing problems with your interface.

9-3 Status Bytes

The Prophet-5 never volunteers DATA FROM, it only transmits when prompted by the sequencer. Communication is initiated by the sequencer transmitting "status" bytes which may or may not signify that data follows. For example, to change programs the sequencer first sends a byte to the Prophet saying that the next byte is the new program number. The Prophet will then wait for this second byte, and change its program accordingly when it is received.

There are 12 unique status bytes. A status byte is simply a unique hexadecimal (H) number. It is distinguished from other bytes merely by being the first which the sequencer transmits to the Prophet as part of any data transfer. The Prophet requires 0 - 1-1/2 milliseconds (worst case) to respond to the status byte interrupt. It will then be ready to receive or transmit data which is formatted and timed as specified below. Generally, while data can be transmitted with spaces of between 1 to 4 ms between bytes without causing errors, you will probably want to operate faster for the most transparent operation. Most of the Prophet's receiving operations are accompanied by a "time-out" which declares an error if data is not received within 4 ms. When such an error is detected, the Prophet simply ignores the received data and resets to wait for another status byte. So if your data arrives too late, or you accidentally send more data than needed, the Prophet may interpret the data as a status byte.

The Prophet will not accept status bytes during its TUNE routine. During TUNE, DATA FROM transmits a BREAK signal to tell the sequencer the Prophet isn't listening. The BREAK is simply a continuous low on DATA FROM. In other words, your receiver will see a start bit followed by no stop bit. The break can therefore be detected by counting at least two framing errors with zero as data received. The BREAK can therefore be used to inhibit the sequencer.

9-4 STATUS 0: SEND KEYBOARD and BANK/PROGRAM BYTES

This status byte is used for the sequencer to record the Prophet's keyboard and "sound" program status. Code 01(H) on DATA TO interrupts the Prophet to read its keyboard. After a 0 - 2-ms (worst-case) delay to respond to the interrupt, the Prophet transmits eight bytes of keyboard information over DATA FROM. As mapped below, 61 of the 64 bits represent key status (three aren't used). 0 means the key is off ("up"), 1 means the key is on ("down"). As shown, the least-significant bit (LSB) of the first byte is the lowest C (CO).

	LSB							MSB
Byte 0	C0	C#0	D0	D#0	E0	F0	F#0	G0
Byte 1	G#0	A0	A#0	B0	C1	C#1	D1	D#1
Byte 2	E1	F1	F#1	G1	G#1	A1	A#1	B1
Byte 3	C2	C#2	D2	D#2	E2	F2	F#2	G2
Byte 4	G#2	A2	A#2	B2	C3	C#3	D3	D#3
Byte 5	E3	F3	F#3	G3	G#3	A3	A#3	B3
Byte 6	C4	C#4	D4	D#4	E4	F4	F#4	G4
Byte 7	G#4	A4	A#4	B4	C5	X	X	X

After sending the eight keyboard bytes the Prophet sends a byte which contains the bank and program number. This byte's format is that the least significant three bits are the PROGRAM number; 0 corresponds to program number 1, 7 corresponds to program number 8. The next three bits are the BANK number; 0 is bank 1, 4 is bank 5. (The two most significant bits aren't used.)

These nine bytes follow close on one another. The delay between keyboard bytes 0 and 1 is 150 us. The time between the remaining eight bytes is a uniform 36.4 us. The sequencer receiver must be ready to receive this data with the required speed, or an overrun error will occur in the sequencer. Note that it is also a good idea to insert "time-outs" in your receiver software so your system is not hung-up waiting for bytes which it somehow may have missed.

You will have to format this data in RAM for your particular requirements. For example, since these bytes only tell the sequencer what keys are being held when it asks, in order to create timing information the sequencer will have to continually sample the Prophet's keyboard and compare to find out when keys go on or off.

9-5 STATUS 1: SEND ACK and RECEIVE KEYBOARD and BANK/PROGRAM BYTES

This status is used for the sequencer to play the Prophet's keyboard and select programs. When code 02(H) is received, the Prophet processes the interrupt (again, for up to 2-ms, worst-case). When it is ready to receive eight keyboard bytes and a program byte, it acknowledges the sequencer's request by sending the "ACK" code 36(H). The sequencer then transmits the keyboard and program bytes in the format discussed under STATUS 0.

For the most transparent operation, you will want a minimum of time between bytes transmitted to the Prophet. The faster the transfer, the truer the timing will be. Some specific timing figures may be of use. For example, the Prophet's scan time (for each program loop) is 6 ms, or 11 ms if controls are being used. This means there is a worst-case delay of 11 ms between a key being pressed and its being heard or recorded. This is not normally detectable in the Prophet. However, sequencing adds new timing concerns, since the Prophet waits for the transfer to be completed before continuing its loop. With a 625 kHz clock, 9 serially-formatted bytes will take only 158.4 us (1.6 us X 99 bits). But if they are spaced 1 ms apart, the whole transfer will about double the worst-case loop time. It is more reasonable to use the fastest clock possible, and allow up to 100 us between bytes. This will have a negligible effect on the Prophet's loop.

The Prophet is protected from being "hung-up" by extremely slow or nonexistent data. Its time-out software declares an error and ignores the whole message if more than about 4 milliseconds elapses between bytes.

When the message is complete, the Prophet places this data into its "Scratchpad" RAM table, playing the notes as if they came from its own keyboard. Even while receiving from the external sequencer the Prophet's keyboard remains active and can be used normally (unless the sequencer TRANSPOSE function is enabled, see STATUS 2). Of course you still have a five-voice maximum. So if you, for example, play on the keyboard while the sequencer is playing, you will "steal" voices from the sequence.

If no program change is desired, you can either transmit the last program number, or the code FF(H) which the Prophet simply ignores. Except for the FF code, the Prophet will sense an error if either of the two MSBs of the program byte are set.

NOTE. Be sure the Prophet is switched to PRESET mode when you want to change programs.

(Status B can be used for changing the program only. Status E can be used for receiving "short" keyboard data. See below.)

9-6 STATUS 2: TRANSPOSE ON

This status byte is used to enable the sequencer transpose function. Once the Prophet receives code 04(H), you can transpose the entire playback sequence over a four-octave range by just hitting a key between C0 and C4 on the Prophet. The transposition is equal to the interval between C2 and the key played. For example, to transpose down a fifth, hit F1. To transpose up a major seventh from the original key, hit B2. To transpose back to the original key, hit C2.

9-7 STATUS 3: SAVE TO TAPE

This status byte is used to extract the contents of the Non-Volatile program RAM from the Prophet, without using the independent CASSETTE interface. Organized as 40 24-byte programs, NV RAM uses 960 of its 1024 (1K) bytes. The least-significant seven bits of each byte represent a programmable pot setting of 0 -127 steps, while the MSB represents a switch setting (1=on, 0=off). The Prophet has another area of RAM called "Scratchpad" in which the current status of the machine is registered. When selecting a program in PRESET mode, a set of 24 bytes is transferred from NV RAM to the Scratchpad, with the "pot" bits filling the pot table and the switch bits being regrouped into the switch status table. Here is how the pot and switch bits are grouped in each NV program:

	Switch Bit (7)	Pot Bits (0-6)
Byte 0	OSC A PULSE	FILT ATK
	OSC A SAW	FILT DEC
	OSC A SYNC	FILT SUS
	OSC B SAW	FILT REL
	OSC B TRI	AMP ATK
	OSC B PULSE	AMP DEC
	OSC B KBD	AMP SUS
	UNISON	AMP REL
	POLY-MOD FREQ A	FILTER CUTOFF
	POLY-MOD PW A	FILT ENV AMT
	POLY-MOD FILT	MIX OSC B
	LFO SAW	OSC B PW
	LFO TRI	MIX OSC A
	LFO SQUARE	OSC A PW
	FILT KBD	MIX NOISE
	RELEASE	FILT RESONANCE
	W-MOD FREQ A	GLIDE
	W-MOD FREQ B	LFO FREQ
	W-MOD PW A	W-MOD SOURCE MIX
	W-MOD PW B	P-MOD OSC B
	W-MOD FILT	P-MOD FILT ENV
	OSC B LO FREQ	OSC A FREQ
	X	OSC B FREQ
Byte 23	X	OSC B FINE

For use with this interface, the Prophet maintains a pointer to NV RAM addresses which allows implied addressing. The pointer initially indicates the first NV RAM address. Whenever the Prophet receives a code 08(H), it outputs the NV RAM byte currently being pointed to, then increments the pointer. Therefore to read all of the NV RAM, the sequencer will have to supply exactly 1024 STATUS 3 requests. (This will leave the pointer reset at the NV RAM beginning address again.) To access specific programs, you can send the number of STATUS 3's required to increment the pointer to the desired starting address, and simply ignore the data the Prophet returns.

Any detected error resets the NV RAM pointer to the first address.

9-8 STATUS 4: LOAD FROM TAPE

This status byte is used to initiate a loading of NV RAM. When the Prophet receives code 10(H), it sets itself to TAPE READ mode, in which it expects to receive exactly 2048 bytes. This will be the entire 40-program data block sent twice (without interruption). The first byte received will be placed in the NV location indicated by the pointer. The Prophet will not recognize status bytes again until all 2048 bytes have been received, or an error occurs. The error clears TAPE READ mode and resets the NV pointer to the first NV address.

To load NV RAM, the Prophet's back panel RECORD switch must be ENABLED.

9-9 STATUS 5: CLEAR TRANSPOSE

Code 20(H) turns off the TRANSPOSE function enabled by Status 2. It also returns the sequence to its original key.

9-10 STATUS 6: INITIALIZE SEQ LOWER PROGRAM

This status byte 40(H) was inherited from the Prophet-10 but should not be sent to the Prophet-5.

9-11 STATUS 9: DISABLE TUNE

Code 09(H) is used to disable the Prophet's TUNE switch. An ideal application would be for the sequencer to disable TUNE before executing a LOAD FROM TAPE operation (STATUS 4).

9-12 STATUS A: ENABLE TUNE

Code 0A(H) reverses STATUS 9, to allow the Prophet to be tuned. This code doesn't start the TUNE routine, it just enables you to hit the switch.

9-13 STATUS B: RECEIVE PROGRAM CHANGE

Code 0B(H) prepares the Prophet to change programs, without the Prophet sending an ACK as with STATUS 1. The program byte has the format described under STATUS 0, and should follow STATUS B after 2 milliseconds. If it arrives before 2 ms, an overrun error may occur. If it doesn't arrive within 4 ms, the Prophet will then expect to be receiving status bytes again.

9-14 STATUS C: SYSTEM CONNECT

This status byte is best used for initial testing of your system hardware. The Prophet responds to code 0C(H) by sending an AA(H). The sequencer thus learns that the Prophet is connected and listening.

9-15 STATUS E: RECEIVE SHORT KEYBOARD DATA

This status byte is similar to STATUS 1, except that the keyboard data is limited to seven bytes (56 notes), and there is no program byte. There is also no ACK. In short, the sequencer ideally sends code 0E(H), waits 2 ms, then sends seven bytes at 100-us intervals. There is a 4-ms timeout.

SECTION 10

REVISION 3.1 and 3.2 DOCUMENTS

10-0 DOCUMENT LIST

D	SD341C	Rev 3.1 PCB 3 CPU, MEMORY (1/4)
E	SD342B	Rev 3.1 PCB 3 DAC, ADC, TUNE, SEQ, CASS BUS DRIVERS (2/4)
N	SD541A	REV 3.1 PCB 5 POWER SUPPLY
	BD051A	REV 3.2 INTERCONNECT DIAGRAM
	PP351	Rev 3.2 PCB 3 PARTS ID
D	SD351D	Rev 3.2 PCB 3 CPU, MEMORY, USART (1/4)
E	SD352C	Rev 3.2 PCB 3 DAC, ADC, TUNE, SEQ, CASS, BUS DRIVERS (2/4)
G	SD354A	Rev 3.2 PCB 3 WMOD, MASTER SUMMERS (4/4)
	PP551A	Rev 3.2 PCB 5 PARTS ID
N	SD551A	REV 3.2 PCB 5 POWER SUPPLY

U311 Z-80 CENTRAL PROCESSOR UNIT

U326 5MHz CLOCK XO12C

½U325 7474

R310 330

2.5MHz CLOCK

C309 C310 C313 .1

R354 100K

½U321 74LS02

-INT -RESET

BACK-UP BATTERY BT301 2.9V

D302 D303 D304 IN914 IN4002

D301 IN914

G303 2.2 10V

C302 10 10V

R301 100K

½U309 74C02

-PWR ON

R303 75K

R302 15K

+22V +5.6V

TO CONTROL PANEL

P201 J301

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

DATA BUS

U327 14504

½U328

DBHI0 DBHI1 DBHI2 DBHI3 DBHI4 DBHI5 DBHI6 DBHI

DATA BUS LEVEL SHIFTER

U318 74LSI38

MEMORY ADDRESS DECODER

-TIMER -RAM 1 -NV RAM -ROM 2 -ROM 1 -ROM 0

(ALL)

-IORQ -RD -WR

INPUT PORT DECODER

½U320 74LS00

½U321 74LS02

U319 74LSI38

-CSI0 -CSI1 -CSI2

-CSOL0 -CSOL1 -CSOL2 -CSOL3 -CSOL4 -CSOL5

LOW-VOLT OUTPUT PORT DECODER

ADDRESS BUS LEVEL SHIFTER

½U328 14504

U329 14556

-CSOH0 -CSOH1 -CSOH2 -CSOH3 -CSOH4 -CSOH5 -CSOH6 -CSOH7

HI-VOLT OUTPUT PORT DECODER

½U343

½U310 74LS00

U312 U313 U314 2716

ROM 0 ROM 1 ROM 2

U316 U317 2114

SCRATCHPAD MEMORY

U315 8253

TIMER / COUNTER (SEE ALSO E)

ADDRESS BUS

½U382 74LS00

½U320

U383 U384 4334

-NV WR

S3 RECORD EN DIS BACK PANEL

ENA REC

NON-VOLATILE PROGRAM MEMORY

SPARES: ½U382

POWER DETECTOR

U372 78M05C

POWER DISTRIBUTION

+5d +15d -15a

C317 C321 C323 C354 C353 C370

NOTES:

1. U309 IS POWERED BY BT301 WHEN POWER SUPPLY IS OFF
2. VERSION B.V9.1
3. VERSION I.V9.1
4. NOT USED
5. MAY BE A JUMPER
6. JUMPER FOR 2.32 (OUT +5V AS INDICATED IN BOARD)

LAST	NOT USED
BT301	
C386	C307, C308
D319	
J302	
P304	
Q303	
R345	
TP306	
J384	U301-U384

			SEQUENTIAL CIRCUITS INC
			PCB 3 CPU, MEMORY, I/O INTFC
			DRN D 10003
	ROM & RAM CHANGES		DWN Jay Antonet 4/4/80 SD341 REV 3.1
7/9/80	29 C386 ADDED		APP
	21 POWER DETECT		MGR S Jamison SHEET 1 OF 4
DATE	REVISION		

DAC LOW BIT LATCH
DAC HIGH BIT LATCH
U336
U337
U342
U343
U344
U345
U346
14174
4049
4013
DAC
DAC 71-CSB-I
V REF
GAIN ADJ
DAC GAIN
R333 100K 20-TURN
R329 100K 1%
C359 .01µF
(651µV)
(1.302mV)
(2.604mV)
(5.208mV)
(10.42mV)
(20.83mV)
(41.67mV)
(83.33mV)
(166.7mV)
(333.3mV)
(666.7mV)
(1.333V)
(2.667V)
(5.333V)
15 MSB
15 LSB
SPARES
2/6 U343
TLO82
LM339
1/6 U364
1/6 U365
DAC BUFFER
U347
LF356
R330 332 n 1%
C358 120PF
R334 5K
ADC GAIN
R335 18.2K 1%
R336 200K 1%
C356 2.2µF
I OUT
RFB
Vdac
GND
U355/56/57-3
P304
CASSETTE IN
J9
BACK PANEL
J11 P302
CASS IN
J3
SEQ GATE IN
U323
MISC INPUT BUS DRIVER
14503
CASS CPR
LM339
R340 4.99K 1%
R341 10K 1%
R342 301K 1%
R343 301K 1%
R344 200K 1%
R346 10M
R337 4.99K 1%
C361 .02µF
D305 IN914
.93V
.94V
J8 REL FT SW
BACK PANEL
R312 100K
R313 100K
R315 100K
R318 100K
EXT GATE BUFFER
C316 2ms DELAY FOR CV SLEW
1/6 U331
U330
4013
-EXT GATE EN
DELAY FOR CV CONV
13V TO 5V LEVEL TRANSLATOR
74LS02
1/4 U321
P304
GATE
ENA REC
FF STATUS
TUNE COUNTER
TUNE MUX
TUNE FF
"FAKE CLOCK"
74LS74
1/2 U322
MISC LATCH
-CSOL4
U332
-FF CL
FFP
FFD
CNTR EN
RESET
R316 2K
C315 .1
R317 4.7K
R324 100K
C351 .0056µF
R323 22K
1/6 U315
COUNTER 0
CYCLE COUNTER (ONE SHOT)
8253
P302 J11
J10
C352 .1µF
CASSETTE OUT
C311
COUNTER 2
TOTAL TIME COUNTER
COUNTER 1
A-440 DIVIDER
1/6 U328
4504
440 SEL
A-440
2.5 MHz
DBUS
ADC INPUT BUS DRIVER
U324
ADC LO
ADC HI
OSC SCALE
TP301
M TEST
TP304
TP306
R307 100K
R309 2K
R314 4.7K
R355 100K
R305 4.7K
ADC CPR
R370 15K
R371 562K 1%
R369 332 1%
R368 332 n 1%
R366 562K 1%
R367 15K
D306 IN914
D307 IN914
ADC +613mV
ADC OV
ADC -606mV
ADC +34mV
ADC -34mV
2/6 U365
1/6 U371
4016
SEQ CV
J302
SEQ OFFSET
R385 100K
R390 1M
R389 1K
R386 10K
R391 30.1K 1%
R388 249K 1%
D314 IN914
-8.6mV
-3.7mV
SEQ SCALE
1/6 U374
LM348
C374
C373
J2
SEQ CV IN
R396 470
EN SEQ CV
U339-2
U340-12
U339-10
U319-10
U319-11
U311-26
U325-9
U329-10
U329-9
U311-16
S3
J302 Vmux
1 BIT EQUIVALENCIES
2 ONLY USED FOR OSC CVs
3 VOLTAGE READINGS WITH ALL POTS SET TO 0 AND U364-7 GROUNDED
SEQUENTIAL CIRCUITS INC
PCB 3 DAC, ADC, TUNE, SEQ, CASS
SD342
1000 3.1
SHEET 2 OF 4
5/7/80 20 EXTEND SEQ SCALE

P1
115/230 VAC
GREEN
BLACK
WHITE
S1
POWER
F1
3/4 A SLO-BLO
(230V: 1/2 A S-B)
S2
LINE SWITCH
230V
115 V
T1
2 x 115V
36VCT, 2.8A
TB501
RED
BLACK
RED
D502
D501
D503
D504
MR501
D506
MR501
C504
2200µF
front view
U502
LM340T5/7805
D505
IN4002
C505
2.2µF
R506
47
U505
LM317T
C510
6300µF
R505
243 1%
C508
2.2µF
C509
10µF
25V
R507
2.55K 1%
R508
200
+15
TRIM
TP501
U501
LM337T
C503
6300µF
R503
121 1%
C502
2.2µF
C501
10µF
25V
R502
1.24K 1%
R501
200
-15
TRIM
TB502
J11
WHITE/ORANGE
+V(+22V)
RED
5.6V
YELLOW
+15V
WHITE
-15V
BLACK
GND
BLACK
GND
LAST
NOT USED
C510
C506,C507
D506
R508
R504
TB502
TP501
U505
U503, U504
SEQUENTIAL CIRCUITS INC
PCB 5 POWER SUPPLY
SD541
REV 3.1
49
DATE
REVISION

TOP PANEL ASSEMBLY
SA1 KEYBOARD
R1 PITCH
R2 MOD
WHEEL BOX
W1 KEYBOARD CABLE 16-WIRE RIBBON
J13
WHEEL CABLE 6-WIRE TWISTED
J201
P201
PCB 2 — LEFT CONTROL PANEL
W201 PCB 1/2 INTERCONNECT 40-WIRE RIBBON
TB201
TB101
PCB 1 — RIGHT CONTROL PANEL
16-PIN DIRECT
P202
6-PIN DIRECT
P301
J12
P305
J15
J301
PCB 3 — COMPUTER BOARD
P304
P303
P302
J11
J402
J302
P401
W2 PCB 3/4 INTERCONNECT 60-WIRE RIBBON
PCB 4 — VOICE BOARD
TB401
P402
J14
BOTTOM PANEL CABLE 20-WIRE TWISTED
VOICE POWER CABLE 3-WIRE TWISTED
SHIELDED AUDIO CABLE
BOTTOM PANEL ASSEMBLY
S1 PWR
T1 TRANSFORMER
J16 ANALOG
J17 DIGITAL
PCB 5 — POWER SUPPLY
TB502
-15 G G +5 -5 +12 +15 +V
F1 FUSE
S2 115/230
P1
TB501
J1 AUDIO OUT
SEQUENCER INTERFACE
J2 VOLTAGE
J3 GATE
IN
J4 VOLTAGE
J5 TRIGGER
OUT
CONTROL VOLTAGE IN
J6 FILTER
J7 AMPLIFIER
J8 RELEASE FOOTSWITCH
CASSETTE
J9 IN
J10 OUT
RECORD
S3 ENABLE
DISABLE
CHASSIS
LAST | NOT USED
F1
J17
P1
R2
S3
SA1
T1
W2
SEQUENTIAL CIRCUITS INC
INTERCONNECTION
D
1000.3.2
BD051
SHEET 1 OF 1
REVISION
DATE

CENTRAL PROCESSOR UNIT

Z-80

CLOCK

X012C 5MHz CLOCK OSC

DATA BUS

ADDRESS BUS

TO CONTROL PANEL

MEMORY ADDRESS DECODER

74LS138

DATA BUS LEVEL SHIFTER

14504

ADDRESS BUS LEVEL SHIFTER

INPUT PORT DECODER

LOW-VOLT OUTPUT PORT DECODER

HI-VOLT OUTPUT PORT DECODER

14556

GATE 5 EN

-RESET

-CLR INT

-IORQ

-RD

-WR

-NV WR

-PWR ON

BACK-UP BATTERY

BT301 2.9V

POWER DETECTOR

POWER DISTRIBUTION

NON-VOLATILE PROGRAM MEMORY

ROM 0

ROM 1 (NOT USED)

ROM 2 (NOT USED)

SCRATCHPAD MEMORY

TIMER / COUNTER (SEE ALSO E)

USART

SPARES:

NOTES:

1. U309 IS POWERED BY BT 301 WHEN POWER SUPPLY IS OFF
2. VERSION PROPHET 9.3
3. MAY BE A JUMPER
4. JUMPER FOR 2716 (CUT A11 AS INDICATED ON BOARD)

LAST	NOT USED
BT 301	
C386	C307, C308
D320	
J302	
P305	
Q312	Q309
R3173	R316-R318

LAST	NOT USED
TP306	
U386	U301-U308
W301	U315/14

SEQUENTIAL CIRCUITS INC

PCB 3 CPU, MEMORY, I/O INTFC

SD351

REVISION	DATE	DWN	APP
GATE 5 MOD	7/29/80		
ROM & RAM CHANGES			
C386 ADDED	7/6/80		
POWER DETECT	2/1/79		

SHEET 1 OF 8

	SEQUENTIAL CIRCUITS INC
TITLE	PCB 3 DESIGNATOR MAP
DSN	SIZE D · MODEL No. 1000.3.2
DWG	DOCUMENT No. PP351
APP	
ISS	SHEET 1 OF 1

REVISION LTR	DATE	REVISION
J		
H		
G		
F		
E		
D		
C		
B		
A		

DAC LOW BIT LATCH

DAC HIGH BIT LATCH

DAC 71-CSB-I

DAC

DAC GAIN

DAC BUFFER

ADC GAIN

TUNE FF

MISC LATCH

SEQ OFFSET

SEQ SCALE

CASS CPR

ADC CPR

MISC INPUT BUS DRIVER

ADC INPUT BUS DRIVER

OSC SCALE

COUNTER 8 CYCLE COUNTER (ONE SHOT)

COUNTER 8 TOTAL TIME COUNTER

COUNTER 1 A-440 DIVIDER

SPARES:

1/6 U343

1/6 U364

1/6 U365

(1) BIT EQUIVALENCIES

(2) ONLY USED FOR OSC CVs

(3) VOLTAGE READINGS WITH ALL POTS SET TO 0 AND U364-7 GROUNDED

7/29/81	69	GATE 5 MOD	
5/7/80	20	EXTEND SEQ SCALE	
DATE		REVISION	

SEQUENTIAL CIRCUITS INC

PCB 3 DAC, ADC, TUNE, SEQ, CASS

DRN D — 1000.3.B

SD352

SHEET 2 OF 4

G

J7 AMPLIFIER CV IN — BACK PANEL — J11 — P301 — W201 W101 — J302 P202 VOL IN — VOL OUT — P304 — P401 VOL CV — R345 100 — +5a — R113 VOLUME 100K

R1 PITCH WHEEL 100K — WHEEL PANEL — J12 — P301 — R3106 4.7K — +15V — R3100 100K 1% — D316 D315 D314 IN914 — PW DEADBAND

R3129 P-WH PITCH WHEEL TRIM 10K — -15V — NC

R104 MASTER TUNE 100K — +5a — FRONT PANEL — P202 J302

U358-5 F -TUNE

U370 4016 — R3102 100K 1% — D317 IN914 — R378 24.9K 1% C387 C368 — R377 1M 1% — R376 2.21M 1% — U367 LM348

P305 R3170 100K 1% — REMOTE V PWHEEL — D320 IN914 — U377 4016

U379 4066 — TLO82 B U373 — R382 100K 1% — R3117 1M

U333-13 F WMOD FREQ A S — U371 4016 — W-MOD — R3104 182K 1% — D313 IN914

R3126 50K — Q309 AD620 — GLIDE — R3124 100K — U358-7 F GLIDE CV — R3125 2.7K — R3123 100K

U380 TLO82 B — C379 — C377 — C376 .1uF mylar 5% — R3121 4.7K

U381 3280 — D319 D318 IN914 — U349-1 F UNISON CV R3122 4.7K — NC

P305 R3165 150K — REMOTE V MOD — R3166 150K — R3168 100K 1% C388 — R3119 154K 1% — U374 LM348 — Q310 2N4250 — R3163 10K 1% — R3164 20K 1%

R2 MOD WHEEL 100K — WHEEL PANEL — P301 J12

R375 1K — U370 4016 — R3101 100K — C371 — R3100 100K 1%

GLIDE OUT CV (UNI)

OSC A MSUM — R365 100K 1% — R364 100K 1% — R363 100K 1% C364 .01 — U368 LM348 — A SUM — P304 — 22

R339 A OFFSET 100K — R382 10M — R381 10K — R383 100K 1%

U341-1 F OSC B KBD S — U379 4066 — TLO82 B U373 — R387 100K 1% — R3118 1M

U333-2 F OSC B LO FREQ S — U371 4016 — R3105 200K 1%

OSC B MSUM — R358 100K 1% — R359 100K 1% — R360 100K 1% C362 .01 — U368 LM348 — B SUM — 20

R338 B OFFSET 100K — R361 10M — R380 10K — R379 100K 1%

U333-7 F WMOD FREQ B S — U371 4016 — R3103 182K 1% — D312 IN914

U375 5837 — PINK NOISE SOURCE — R395 47K — U374 LM348 — R3119 20K — U378 3280 — R3120 330

R394 300K — R393 100K — C372 .01 — R3116 6.2K — Q307 2N4250 — R3115 3.5K — C378

-600mV — D310 IN914 — R388 1K — C369 .1

U341-13 F FILT KBD S — U369 4016 — J6 FILTER CV IN BACK PANEL — J11 P302 — R374 100K 1%

U333-12 F WMOD FILT S — U369 4016 — R399 13.3K 1% — D311 IN914 — R372 100K 1%

FILT MSUM — R354 100K 1% — R357 100K 1% C365 .01 — R356 261K 1% — R355 100K 1% — U367 LM348 — FILT SUM CV — 14

U360-7 F FILT CTF CV — R352 100K 1% — C367 .1 — R353 10K

U333-5 F WMOD PW B S — U369 4016 — R398 15K — D309 IN914

U360-1 F OSC B PW CV — R349 100K — R373 100K

PW B MSUM — R350 92.3K 1% — R351 100K 1% — U366 LM348 — PW B SUM CV — 15

U333-10 F WMOD PW A S — U369 4016 — R397 15K — D308 IN914

U351-7 F OSC A PW CV — R348 100K — R347 100K

PW A MSUM — U366 LM348 — PW A SUM CV — 16

U359-7 F LO FREQ CV — LFO — U376 3340 — SUM — PW MOD — H SYNC — EXP CV — CF — S SYNC — TCO — TCO — V- — LFM — HI FREQ GND — V+

R3135 6.87K 1% — R3110 10K — R3136 110K 1% — R3134 470 — R3111 2K — C375 .01 mylar — R3112 470K — C385 .01 — R3109 910 — R3107 30.1K 1% — R3108 5.62K 1% — R3138 2.21M 1% — R3139 470 — C384 .01

U334-5 F LFO Λ S — U377 4016 — C380 .1 — R3133 160K — U334-2 F LFO ⎍ S — R3132 200K — R3127 10K — U334-12 F LFO ^ S — R3137 1.62K 1% — C382 .1 mylar 5% — C381 .1

R3128 10K — Q308 2N4250 — R3130 20K — R3146 10K — 4.97V — R3145 5.1K — C383 .1 — R3148 100K — 2.47V — R3147 100K — R3149 1M — 2.39V — R3150 1M

R3168 WHEEL BAL 100K — R3114 3.3K — R3123 3.3K — R3172 75K — R3173 330 — R3171 2.2M — R3170 330 — U381 3280 — R3169 10K — W-MOD BUFFER U374 LM348

SPARES: J12/P301-4 — U379 4066 — NC — 4066 — NC

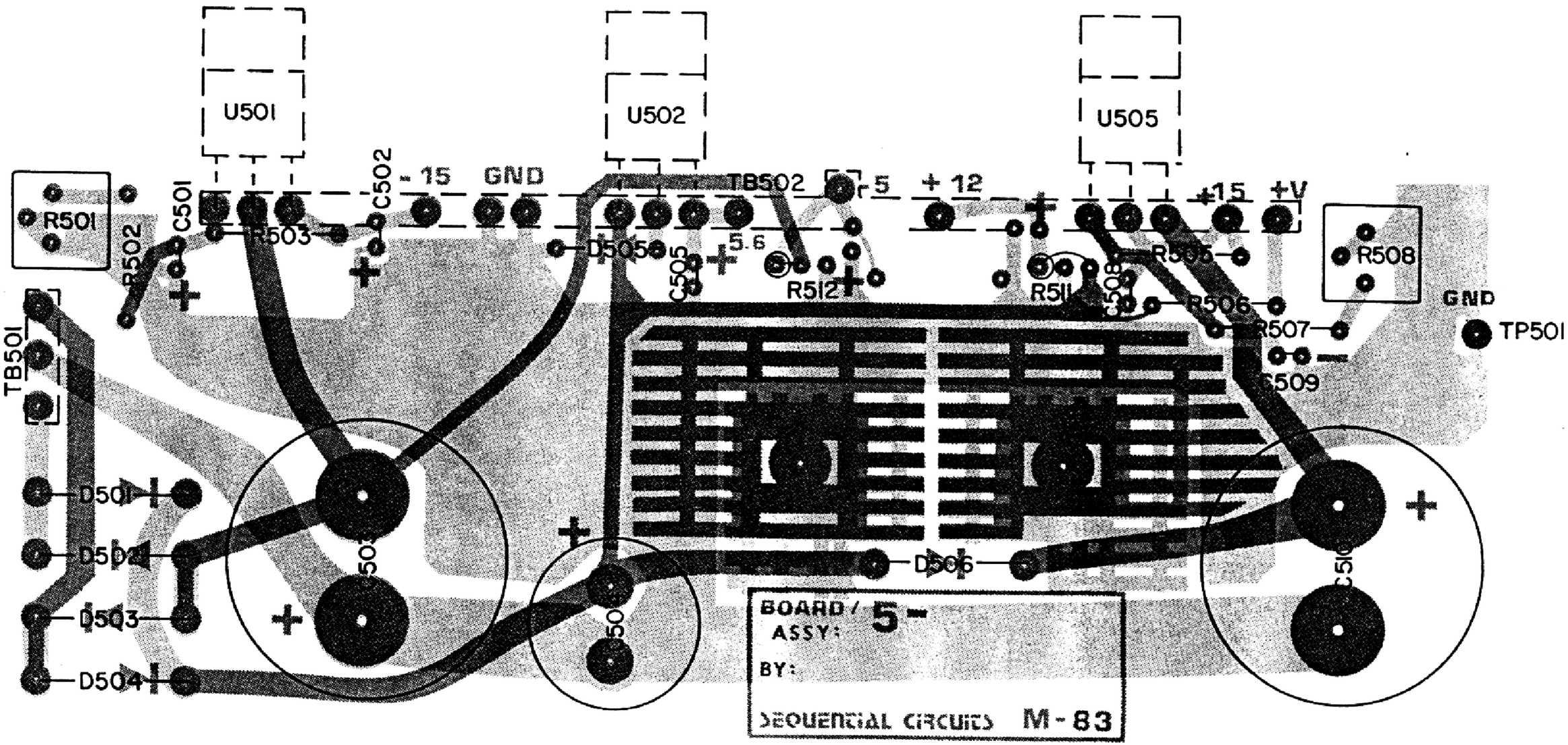
R3141 LFO BAL 100K — R3151 2.2MΩ — R3152 330

Λ B N MATCHED TO 01%

SEQUENTIAL CIRCUITS INC

TITLE PCB 3 WMOD, MASTER SUMMERS

SIZE D — DWG NO 1000.3 — SD354 — REV 3.2 — SHEET 4 OF 4

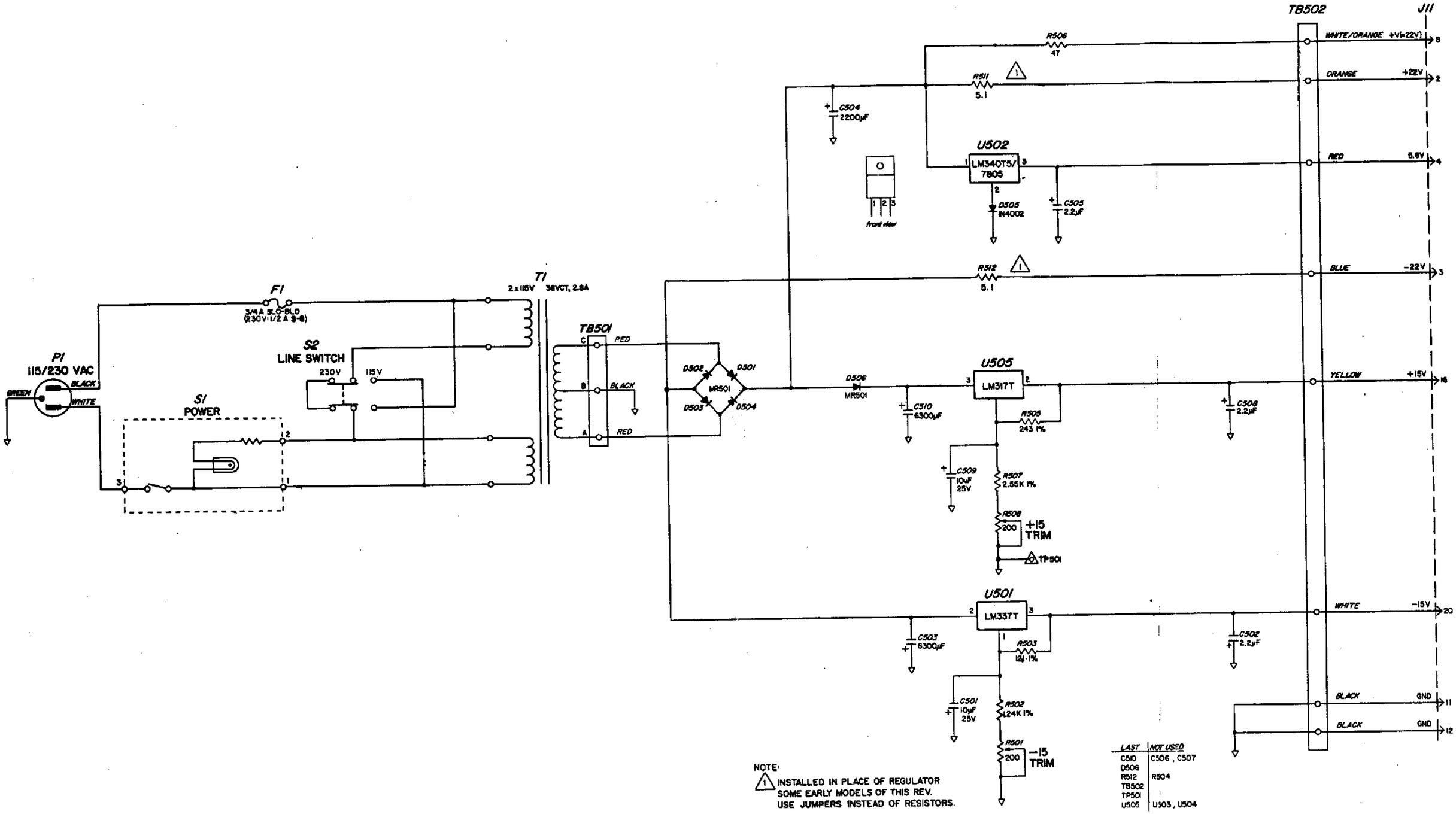


FIRST / LAST S/N	DATE	ECR No	REVISION	LTR
				J
				H
				G
				F
				E
				D
				C
			ADD 2X5.1Ω	B
	10/21/83	36	Remove +12ℓ -5 circuits	A

SEQUENTIAL CIRCUITS INC

TITLE: PCB 5 PARTS ID

DSN	DATE	SIZE: B	MODEL No.: 1000.3.2
DWG D. SIMARD		DOCUMENT No.: PP551	
APP			
ISS S Aung Ceib	9/12/80		SHEET 1 OF 1



NOTE:
⚠1 INSTALLED IN PLACE OF REGULATOR
SOME EARLY MODELS OF THIS REV.
USE JUMPERS INSTEAD OF RESISTORS.

LAST	NOT USED
C510	C506 , C507
D506	
R512	R504
TB502	
TP501	
U505	U503 , U504

REVISION	DATE	APP'D
58 JUMPERS +/-22		

SEQUENTIAL CIRCUITS INC

TITLE: PCB 5 POWER SUPPLY

DRN
CHKD fgabs 4/4/80
APP
MFG S Mayfield 9/15/80

SIZE D | DWG. NO. 1000.3.2 | DOCUMENT NO. SD551 | SHEET 1 OF 1

11-0 INTRODUCTION

This section contains instructions for converting Rev 3.0 or 3.1 Prophets to Rev 3.2. It also presents procedure for Rev 3.0, 3.1, and 3.2 diagnostic computer tests. Finally, there is a trim procedure for the added WHEEL-MOD VCA in Rev 3.2.

11-1 REVISION 3.2 RETROFIT KIT INSTRUCTIONS

Revision 3.2 Retrofit kits can be ordered through the Service Dept. as Model 863. The kit includes:

QUANTITY	SCI P/N	DESCRIPTION
3	M-031	lockwasher
1	M-362	DIGITAL/ANALOG Label
2	R-046	5.1 ohm
1	Z-803	Assembled and Tested PCB 3
1	Z-804	Assembled and Tested Wire Harness

Back Panel Modification

1. Open the Rev 3.0 or 3.1 Prophet as shown in Section 1. Disconnect Power Supply connector P302 and the Audio Cable P402. Set the entire top section aside.

2. Remove PCB 5 Power Supply Board and regulators from back panel. PCB 5 will later be modified.

3. Mark and centerpunch the back panel according to Fig. 11-0.

4. Drill (2) ¼-inch pilot holes.

5. Enlarge the holes to 5/8" using a chassis punch according to the instructions provided by the manufacturer. (Order SCI #Q-064, GREENLEE Chassis Punch #799-3214.)

6. Mount the jacks according to Fig. 11-1. Make sure that the jacks are mounted in the correct locations, which are the 5-pin jack on the right (toward edge) and 4-pin jack on the left. **Note:** To prevent twisting which could damage the wiring, hold the back of the jack with a wrench when tightening the front nut.

7. Install label (M-362) below jacks as shown in Fig. 11-0.

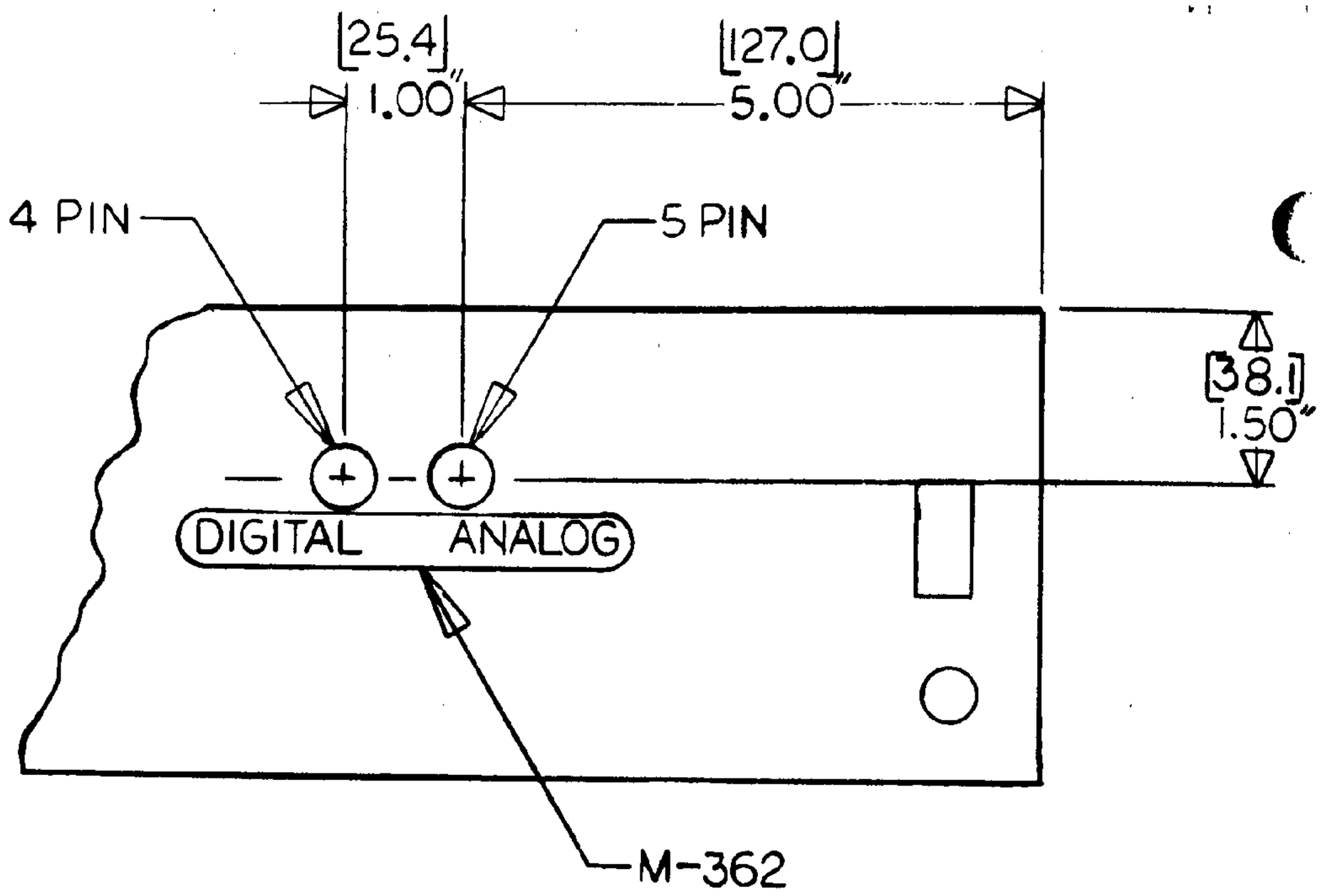


Figure 11-0

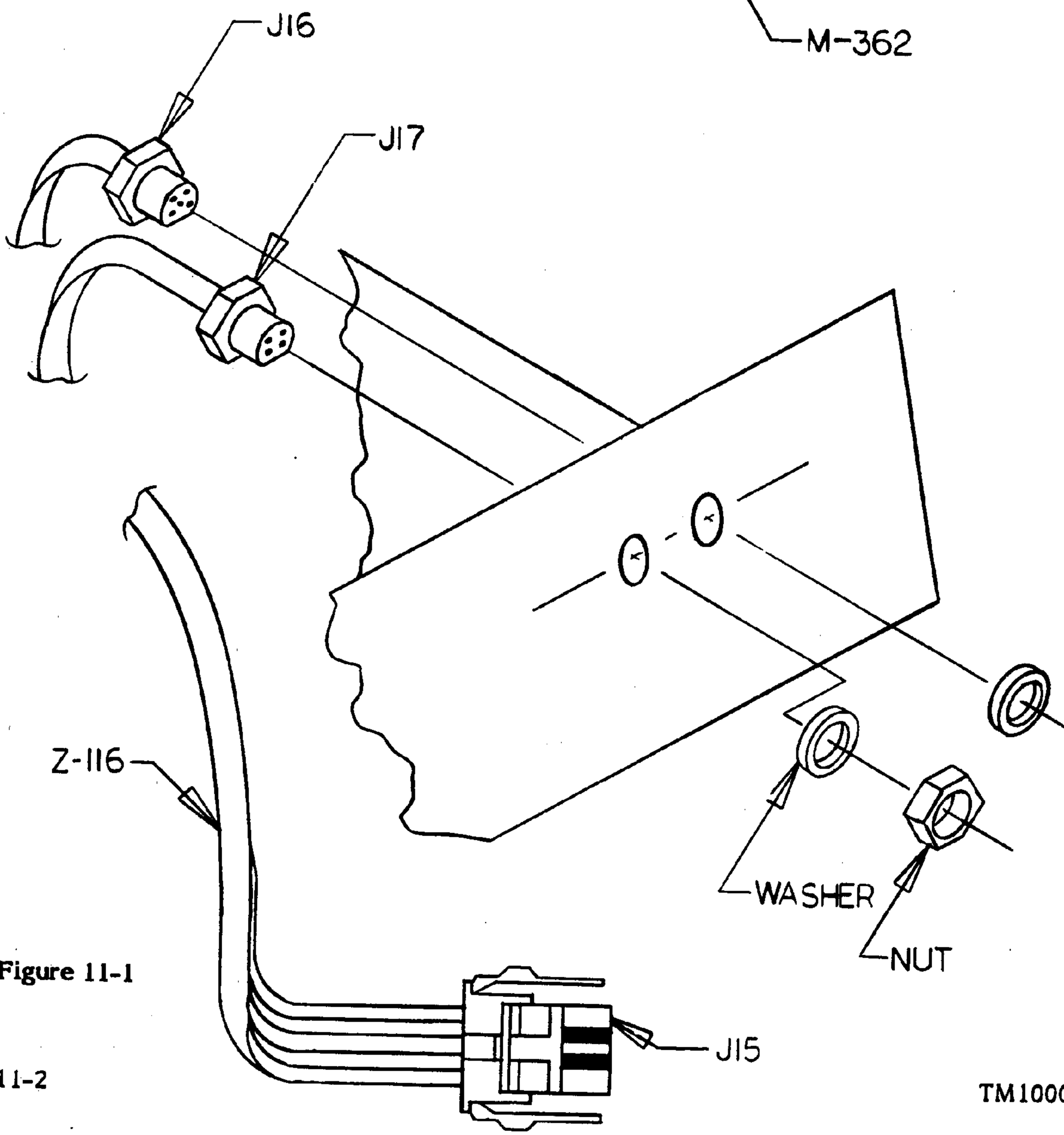


Figure 11-1

PCB 5 Modifications

8. If the Prophet is Rev 3.1, go to step 10.

9. If the Prophet is Rev 3.0, refer to pages 3-22 and 3-23 above, and remove these parts from PCB5: C507 (2.2 uF), U504 (78M12), R504 (1K), C506 (2.2 uF), U503 (7905).

10. Install a 5.1-ohm resistor between holes 1 and 3 of U504. As can be seen on the schematic, this ties +22V to the (formerly) +12V line. (The Rev 3.2 PROM doesn't need +12 or -5V.)

11. Install a 5.1-ohm resistor between holes 2 and 3 of U503. This ties -22V to the (formerly) -5V line.

12. Reinstall PCB5. There have been a few instances of loose regulators producing intermittant problems, usually with tuning. To prevent this, drill out the mounting holes with a #33 bit. Re-install the three remaining regulators, using nylon shoulder washers and adding the provided lockwasher under the #4 nut. Use loctite on threads. Hold nut with wrench and tighten screw with screwdriver tightly (until nylon shoulder washer begins to deform). Check for electrical isolation with ohmmeter.

PCB 3 Replacement

13. Remove the Rev 3.0 or 3.1 PCB 3 referring to pages 1-1 through 1-4.

14. Install the Rev 3.2 PCB 3.

15. Connect J15 9 pin connector to P305 on PCB 3. (For reference, see Rev 3.2 Interconnect diagram in Section 10.)

16. Reconnect remaining cables and check that all connections are tight.

17. Follow the Functional Test Procedures detailed above in pages 4-2 through 4-9.

18. Trim as required (see pages 4-11 to 4-16).

11-2 REVISION 3.0 MEMORY TEST

Rev 3.0 Serial Numbers: 1300-2285, 2424-2451, 2456, 2466, 2477

Software: V.8.0 (1300-1309, 1311, 1312, 1314-1321, 1324, 1328)
V.8.1 (1310, 1313, 1321-1323, 1325-1327, 1329-2285, 2424-2451, 2456, 2466, 2477)

NOTE: Following the appearance of a few Rev 3.0 Prophets which spontaneously put themselves into Edit Mode, the Rev 3.0 has been updated to (post-production) V.8.2, available as a 3-PROM set, SCI #Z-984.

Rev 3.0 Prophet-5s are tested with a special 2708 EPROM which can be ordered as SCI #Z-953.

NOTE. Check that the RECORD switch is ENABLEd, and that user's programs are stored on cassette since the memory tests erase the NV RAM contents.

1. Switch power off and insert PROM in PROM 0 location (U312). (If available, insert factory program PROM PROGS.5 into PROM 1 (U313) location. The test will load NV RAM with programs during section 3).

2. Switch power on. The test will start, indicating the memory section in the PROGRAM display:

1 = Scratchpad RAM
2 = NV RAM
3 = NV RAM load
4 = 8253 Timer
0 = End of test. No failures.

3. If a test fails, the program halts and displays the section number for the problem area. Further tests are not executed until the problem is fixed.

11-3 REVISION 3.1 MEMORY TEST

Rev 3.1 Serial Numbers 2286-2423
Software: V.9.1

Rev 3.1 has the memory test built-in but a simple hardware modification may be required before it can be enabled.

NOTE. Check that the RECORD switch is ENABLEd, and that user's programs are stored on cassette since the memory tests erase the NV RAM contents.

1. First, switch power off. The RAM test program is contained in the standard 2716 software, V.9.1. (NV load similar to Rev 3.0 is provided.)

2. If necessary, on foil-side (or, bottom) of PCB 3, cut trace between U324-10 and ground.

3. See SD342 in Section 10. If not installed, connect R3155 100K pull-down resistor from U324-10 to ground at U324-8.

4. To vector to the internal test program, jumper TP305 (U324-10) to +5V then switch power on. (The test point location is shown on PP351, Section 10). The test will start, indicating the memory section in the PROGRAM display:

1 = Scratchpad RAM
2 = NV RAM
3 = NV RAM load
4 = 8253 Timer
0 = End of test. No failures.

5. If a test fails, the program halts and displays the section number for the problem area. Further tests are not executed until the problem is fixed.

11-4 REVISION 3.2 MEMORY TEST

All Rev 3.2 Prophet-5s have the memory test built-in.

Rev 3.2 2452-2455, 2457-2465, 2467-2476, 2478 and up
Software: V.9.2

Software level V.9.2 has the memory test only. Later-production instruments have software version V.9.3 which prefaces the memory test with a basic CPU test. This routine doesn't use RAM so is useful for seeing if the CPU itself is working and accessing PROM.

NOTE. Check that the RECORD switch is ENABLEd, and that user's programs are stored on cassette or via the Model 1005 Polyphonic Sequencer since the memory tests erase the NV RAM contents.

1. First, switch power off.

2. To vector to the internal test program, jumper TP304 MEM TEST to +5V then switch power on.

3. If software is V.9.3, the Prophet will sequentially flash its LEDs (in the order in which they are wired in the matrix). To exit this mode and start the regular RAM test, press TUNE.

4. The memory test will start, indicating the memory section in the PROGRAM display:

1 = Scratchpad RAM
2 = NV RAM
3 = PROM
4 = 8253 Timer
0 = End of test. No failures.

3. If a test fails, the program halts and displays the section number for the problem area. Further tests are not executed until the problem is fixed.

11-5 WHEEL BALANCE TRIM

1. See para. 4-13 and trim WHEEL-MOD LFO VCA BALANCE, and see para. 4-15 and trim WHEEL-MOD NOISE VCA BALANCE.

2. Switch off all LFO waveshapes.

3. Set WHEEL-MOD SOURCE MIX knob to 0.

4. Advance MOD wheel fully.

5. Probe U374-14, W-MOD Buffer output. (For parts locations, see PP351 in Section 10.)

6. Adjust R3168 WHEEL BAL trimmer to read as close to 0.000V as possible.

REVISION 3.2 COMPONENTS

Changed from Rev 3.0	
R339	R-217
R378	R-110A
R3119	R-175
R3120	R-015
R3153	R-025
Added	
D320	D-005
Q310-12	T-003
R3154	R-011
R3155/6	R-012
R3157/8	R-025
R3159	R-011
R3160	R-010
R3161	R-025
R3162	R-110
R3163	R-108
R3164	R-144
R3165/6	R-077
R3167	R-036
R3168	R-217
R3169	R-012
R3170	R-004
R3171	R-030
R3172	R-022
R3173	R-004
R511/2	R-046

SECTION 13

PROPHET-5 REV 3.3 UPDATE

This modification increases the Prophet-5's program storage capacity from 40 to 120. The update involves adding a jumper to the back of PCB 2 Left Control Panel, adding RAM and some logic to the Rev 3.2 PCB 3 Computer Board, and changing the software. The Update Kit (#Z-205) includes the following parts:

PARTS

CM1000C.2	Prophet-5 Rev 3.3 Op Manual Addendum
I-043	6116 RAM
I-240	74C00 Quad NAND gate
J-017	24-pin DIP socket
Z-994	Prophet-5 software
Z-068	Prophet-5 120-Factory Program Cassette

PROCEDURE

1. Switch power off and disconnect the Prophet from the AC line.

2. Open the box. (For instructions, see Section 1 of Technical Manual TM1000D.)

3. Disconnect and remove PCB 4.

4. Disconnect and remove PCB 3.

5. See Fig. 1 and add the jumpers shown to the back of PCB 2. This ties together the display decimal points (pins 4 and 9) to LD7, pin 33 of TB201, as shown on the Rev 3.3 PCB 2 schematic (attached).

6. The remaining modifications to PCB 3 are illustrated in Figs. 2 and 3, and the Rev 3.3 PCB 3 schematic (attached). First bend out all the pins of the enclosed 74C00 Quad NAND gate, except pins 4, 7, and 14. Solder this device "piggyback" to U309 (74C02) at pins 4, 7, and 14 (Note that U309 is oriented with pin 1 at the upper right).

7. The added 74C00 is designated U387. Jumper U387 pins 2, 1, 14, and 13 in a loop around the end of the IC.

8. Jumper U387-10 and U387-11.

9. Jumper U387-4 to U387-9.

10. Jumper from the feed-through for U311-1 (A11), to U387-5 and -12. It should be possible to do this with one piece of wire.

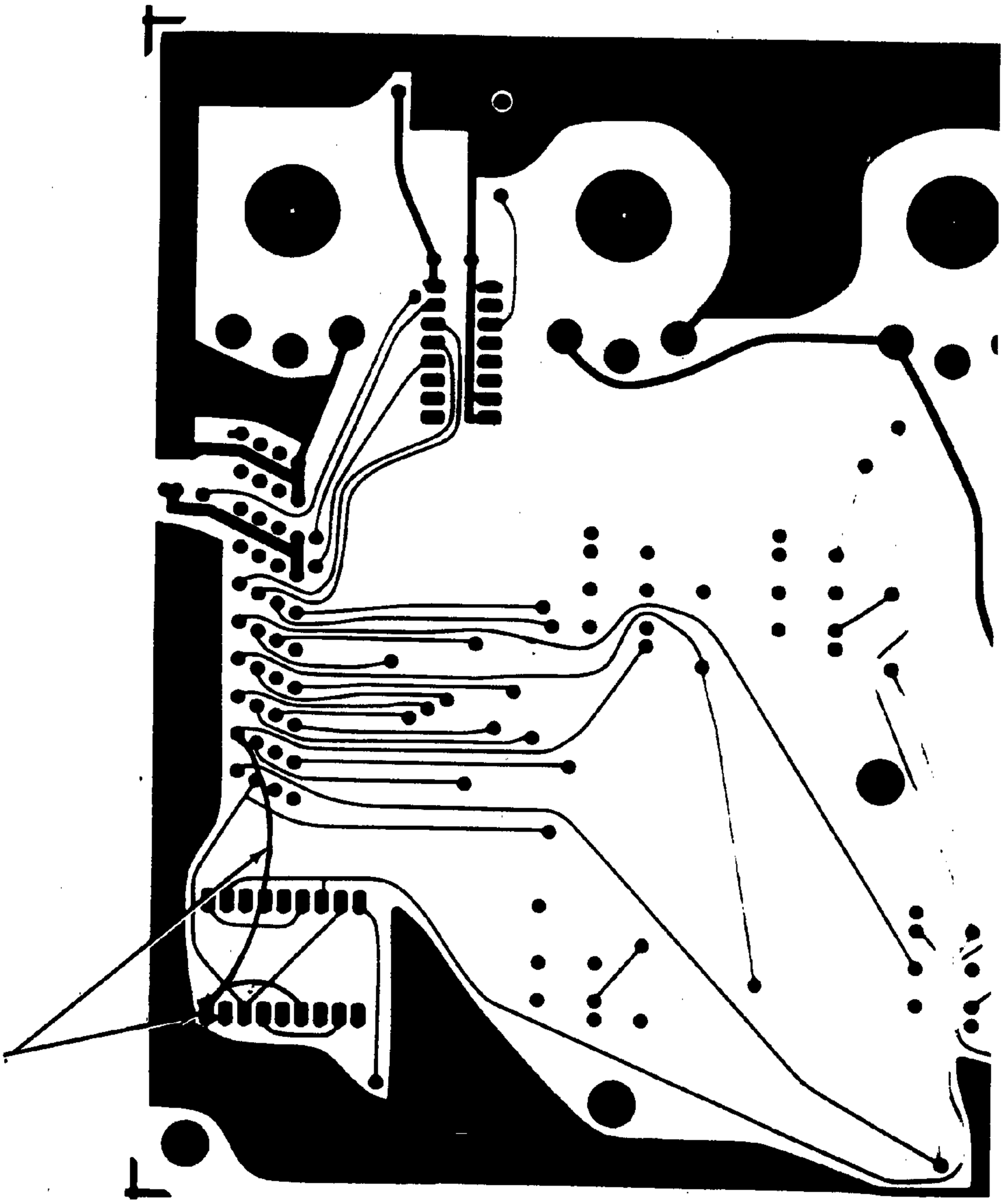


Figure 13-0
PCB 2 BOTTOM MODIFICATION

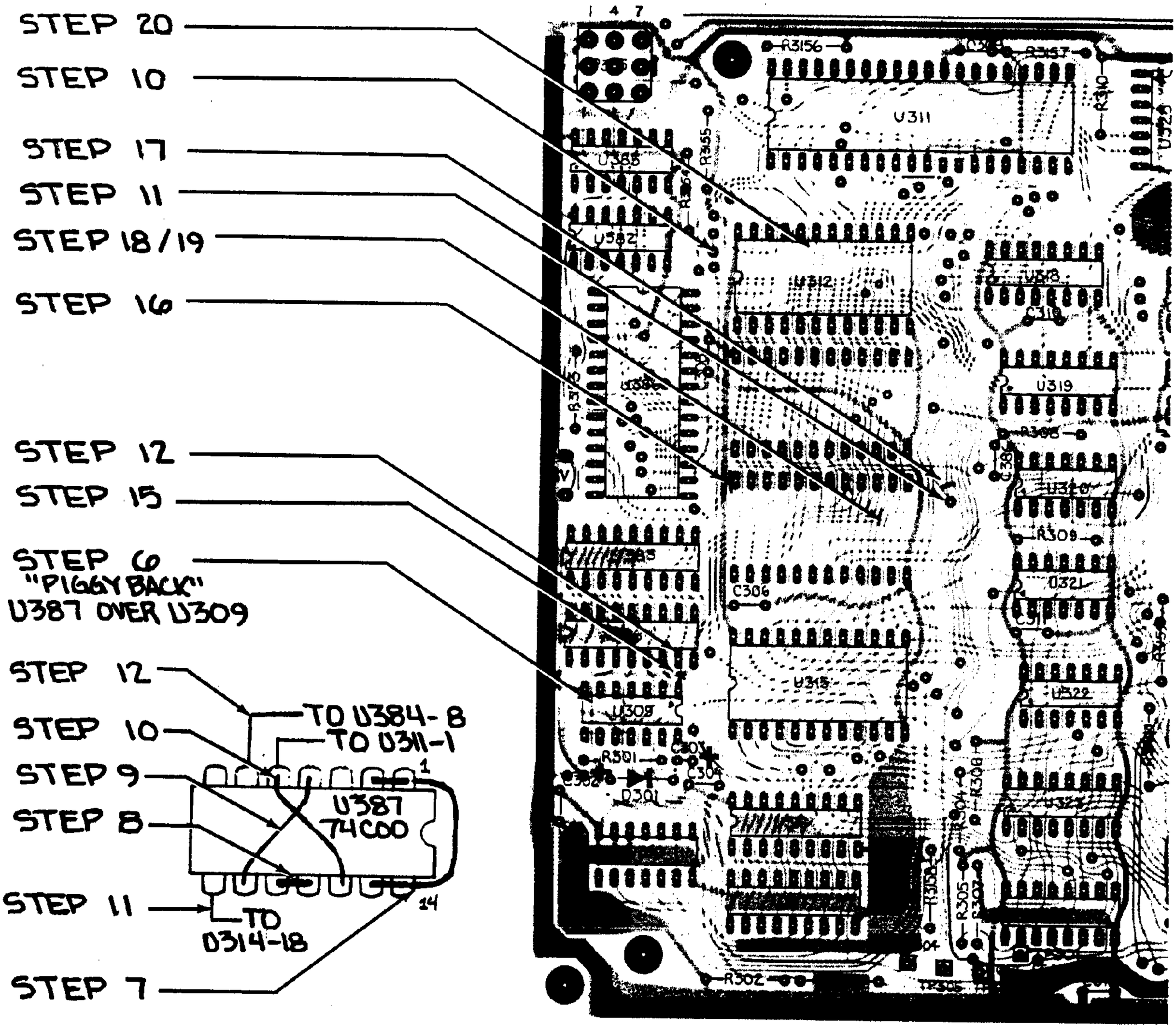


Figure 13-1
PCB 3 TOP MODIFICATION

11. Jumper from the feed-through for U314-18 (-CE), to U387-8.

12. Jumper from U384-8 (-CS), to U387-6.

13. See Fig. 3 (bottom). Jumper U314-24 to U383-18 (Vnv).

14. Jumper U314-21 to U383-10 (-WR).

15. See Fig 2. Cut trace between U384-8 and U309-1.

16. Cut the trace between U314-24 and +5V.

17. Cut the trace from U318-13 (-ROM 2) to U314-18.

18. Install the 24-pin socket in the space reserved for U314.

19. Insert 6116 RAM into U314 socket.

20. Replace software at U312 with version enclosed.

21. Assemble unit and run a functional test.

22. Verify NV operation by recording, and loading (and re-saving) included factory programs to Program Files 2 and 3 with the Cassette Interface. (The Addendum enclosed with the kit explains how to access the new Program Files.)

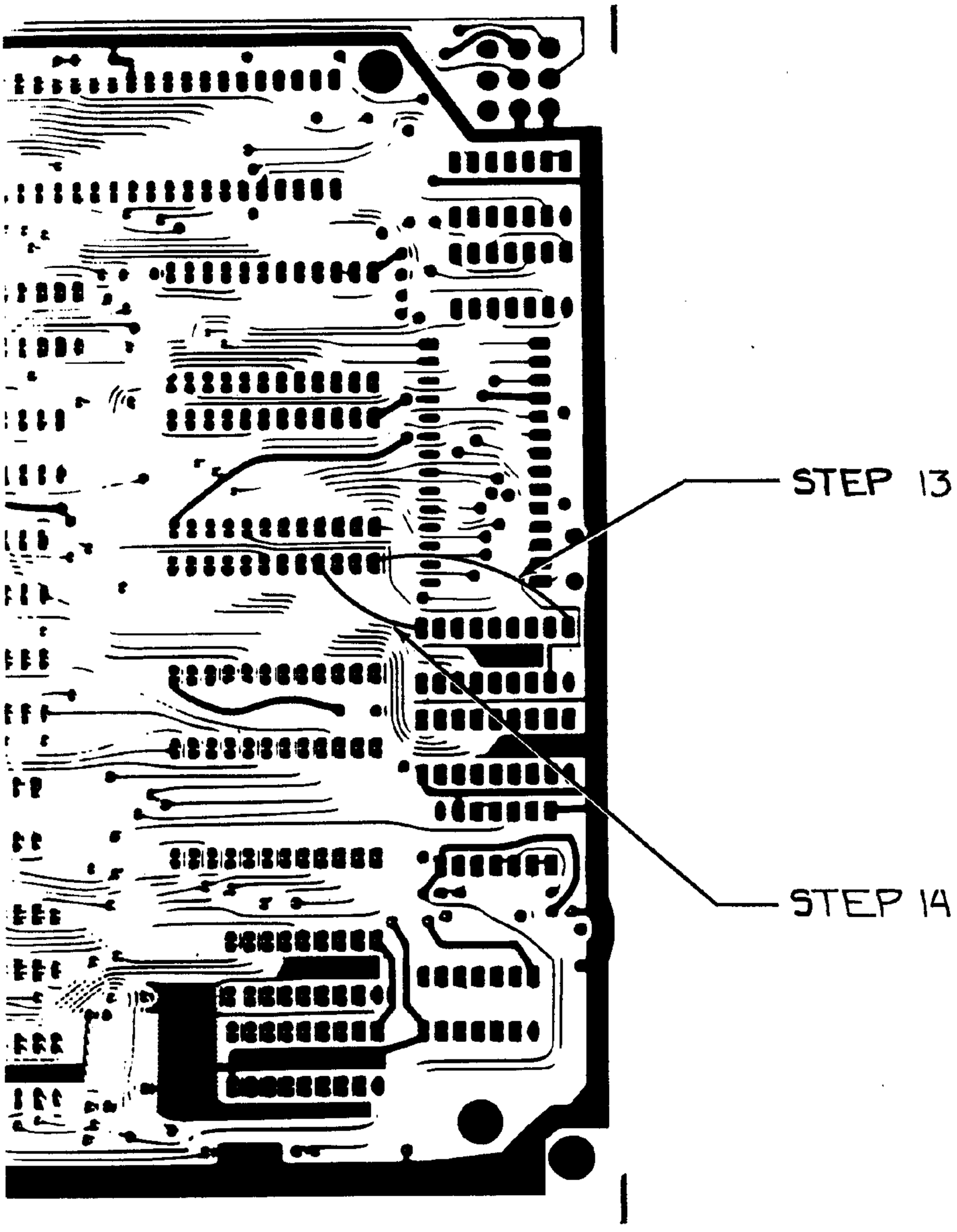


Figure 13-2
PCB 3 BOTTOM MODIFICATION

TB201 TO PCB 1

U204 4042 — QA201 3082 — RA201 39 (all) — LED MATRIX

LR1 LR3 LR4 DS224

LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7

DS205 OSC A ⊓ | DS201 PMOD FREQ A | DS215 WMOD FREQ A | (DS105) PS1 | DS222 RECORD | a1 a2
DS204 OSC A ∧ | DS202 PMOD PWA | DS216 WMOD FREQ B | (DS106) PS2 | b1 b2
DS206 OSC A SYNC | DS203 PMOD FILT | DS217 WMOD PWA | (DS107) PS3 | (DS102) A-440 | c1 c2
DS210 OSC B ∧ | DS207 LFO ∧ | DS218 WMOD PWB | (DS108) PS4 | (DS114) TUNE | d1 d2
BANK PROGRAM 9
DS211 OSC B ∧ | DS208 LFO ∧ | DS219 WMOD FILT | (DS109) PS5 | (DS103) TO CASS | e1 e2
DS212 OSC B ⊓ | DS209 LFO ⊓ | DS213 OSC B LO | (DS110) PS6 | (DS104) FROM CASS | f1 f2
DS214 OSC B KBD | (DS101) FILT KBD | (DS111) PS7 | g1 g2
DS220 UNISON | (DS113) RELEASE | (DS112) PS8 | DS221 PRESET | DP1 DP2

U205 4042 — Q201 2N3904 — -CSOL0 — P201 — LED DRIVER LATCH

U206 2003 — C203 — U208 4042 — U207 4042 — R218 2K

P201 -CSOL1 — LED SINK LATCH

U212 4514 — P201 CSOL2 — SW/KBD ROW DECODER

TB201 TO PCB 1

SWITCH/KBD MATRIX

	SR0	SR1	SR2	SR3	SR4	SR5	SR6	SR7
S0	S205 D205 OSC A ⊓	S204 D204 OSC A ∧	S206 D206 OSC A SYNC	S210 D210 OSC B ∧	S211 D211 OSC B ∧	S212 D212 OSC B ⊓	S214 D214 OSC B KBD	S220 D220 UNISON
S1	S201 D201 PMOD FREQ A	S202 D202 PMOD PWA	S203 D203 PMOD FILT	S207 D207 LFO ∧	S208 D208 LFO ∧	S209 D209 LFO ⊓	(S101 D101 KBD)	(S113 D113 RELEASE)
S2	S215 D215 WMOD FREQ A	S216 D216 WMOD FREQ B	S217 D217 WMOD PW A	S218 D218 WMOD PW B	S219 D219 WMOD FILT	S213 D213 OSC B LO		
S3	(S105 D105 PS1)	(S106 D106 PS2)	(S107 D107 PS3)	(S108 D108 PS4)	(S109 D109 PS5)	(S110 D110 PS6)	(S111 D111 PS7)	(S112 D112 PS8)
S4	S222 D222 RECORD	S223 D223 BANK SELECT	(S102 D102 A-440)	(S114 D114 TUNE)	(S103 D103 TO CASS)	(S104 D104 FROM CASS)		S221 D221 PRESET

J201 J13

C0 C#0 D0 D#0 E0 F0 F#0 G0
G#0 A0 A#0 B0 C1 C#1 D1 D#1
E1 F1 F#1 G1 G#1 A1 A#1 B1
C2 C#2 D2 D#2 E2 F2 F#2 G2
G#2 A2 A#2 B2 C3 C#3 D3 D#3
E3 F3 F#3 G3 G#3 A3 A#3 B3
C4 C#4 D4 D#4 E4 F4 F#4 G4
G#4 A4 A#4 B4 C5

SA1 KEYBOARD

W1 KEYBOARD CABLE NOT SHOWN

½RA202 22K (all)

SW/KBD STATUS BUS DRIVER — ⅔U209 ⅔U210 4503 — R219 2K — P201 -CSI0

SPARES:

½RA202 — RESISTOR PACK ALL 22K

½U209 ½U210 4503

⚠1 S201-21 ARE BLACK
S222/24 ARE GREY
S223 IS ORANGE

⚠2 CONTROLS IN PARENTHESIS ARE ON PCB1

SEQUENTIAL CIRCUITS INC

TITLE PCB 2 CONTROL MATRICES

DSN — DWN — APP — DATE — REVISION — MFG S Jung Lab

SIZE D — DRWG No 1000.3 — DOCUMENT No SD232 — SHEET 2 OF 2

DATA BUS

ADDRESS BUS

NON-VOLATILE PROGRAM MEMORY

CENTRAL PROCESSOR UNIT

MEMORY ADDRESS DECODER

INPUT PORT DECODER

ADDRESS BUS LEVEL SHIFTER

DATA BUS LEVEL SHIFTER

LOW-VOLT. OUTPUT PORT DECODER

HI-VOLT OUTPUT PORT DECODER

TIMER / COUNTER (SEE ALSO E)

POWER DETECTOR

POWER DISTRIBUTION

CLOCK

TO CONTROL PANEL

U311 Z-80

U312 2732 ROM Ø

U313 2732 ROM 1 (NOT USED)

U314 6116 NV RAM1

U316 2114 SCRATCHPAD

U317 2114 MEMORY

U318 74LS138

U319 74LS138

U320 74LS00

U321 74LS02

U325 7474

U326 5MHz CLOCK XO12C

U327 14504

U328 14504

U329 14556

U330-8 GATE 5 EN

U332-1 -RESET

U333-9 -CSOH2

U334-9 -CSOH3

U335-9 -CSOH0

U336-9 -CSOH4

U337-9 -CSOH7

U339-9 -CSOH5

U340-9 -CSOH6

U343 4049

U372 IN 78M05OUT

U382 74LS00

U383 4334

U384 4334

U385 74LS08

U386 USART 2661

U387 74C00

U309 74C02

U323-14 ENA REC

U330-2 -INT

U331-9 -CSOL4

U332-9 -CSOL5

U333-9 -CSOL6

U336-9 -CSOL7

U337-9 -CSOL3

U338-9 -CSOL2

U339-9 -CSOL1

U340-9 -CSOL0

P201 J301

P302 +5.6V

P303 +15a

P305 -15a

P306 +22V

P307 -22V

P309 -NV CS

P310 -PWR ON

P312 -NV WR

P505 DATA FROM SYNTH / DATA TO SYNTH / CLOCK TO SYNTH

D BUS

-IORQ

-RD

-WR

A11

-ROM I

-ROM Ø

-TIMER

-GATE 5 EN

-RAM I

-NV RAM

USART

BACK-UP BATTERY BT301 2.9V

D302 IN914

D303 IN914

D304 IN4002

D305 IN914

D306 IN914

D307 IN914

D308 IN914

D309 IN914

D310 IN914

D311 IN914

D312 IN914

D313 IN914

D314 IN914

D315 IN914

D316 IN914

D317 IN914

D318 IN914

D319 IN914

D320 IN914

D321 IN914

D322 IN914

D323 IN914

D324 IN914

D325 IN914

D326 IN914

D327 IN914

D328 IN914

D329 IN914

D330 IN914

D331 IN914

D332 IN914

D333 IN914

D334 IN914

D335 IN914

D336 IN914

D337 IN914

D338 IN914

D339 IN914

D340 IN914

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NOTES:

1. U309 IS POWERED BY BT301 WHEN POWER SUPPLY IS OFF
2. VERSION PROPHET 9.4
3. MAY BE A JUMPER
4. JUMPER FOR 2716 (CUT ALL AS INDICATED ON BOARD)

LAST	NOT USED	LAST	NOT USED
BT301	-	TP106	U301 - U308
C386	C307, C308	U317	U313
D320		W301	
J302			
P305			
Q312	Q309		
R3174	R316 - R318		

SPARES:

1/4 U309 (74C02)

1/4 U385 (74LS08)

1/4 U387 (74C00)

SEQUENTIAL CIRCUITS INC

PCB 3 CPU, MEMORY, I/O INTFC

REVISION	DATE	BY	DESCRIPTION
21	12/18/81		134 MOD FOR 120 PROGS
20	7/29/81	69	GATE 5 MOD ROM & RAM CHANGES
29	7/8/80		C386 ADDED
21			POWER DETECT

DSN D DWN APP

DOCUMENT NO. SD361

SHEET 1 OF 4

INDEX TO TM1016B

Index Date: 6 Dec, 1982
Index also covers TM1000D.4 (Sections 1-13, 23) and TM1016A (Sections 1-22)

Instrument Codes
Instrument series are coded by model number, followed by a period and the rev level.

1000.1	Prophet-5 Synthesizer, Rev 1 (S/N 1-182)
1000.2	Prophet-5 Synthesizer, Rev 2 (184-1299)
1000.3.0	Prophet-5 Synthesizer, Rev 3 (1300-)
1000.3.1	Prophet-5 Synthesizer, Rev 3.1 (RAM changes)
1000.3.2	Prophet-5 Synthesizer, Rev 3.2 (USART, Analog)
1000.3.3	Prophet-5 Synthesizer, Rev 3.3 (120-program)
1001	Prophet-5 Remote Keyboard
1005	Prophet-5 Polyphonic Sequencer
1010.0	Prophet-10 Synthesizer, Rev 0 (1-329)
1010.1	Prophet-10 Synthesizer, Rev 1
1015.0	Prophet-10 Polyphonic Sequencer, Rev 0 (1-329)
1015.1	Prophet-10 Polyphonic Sequencer, Rev 1 (330-)
1016.0	Prophet-10 with Rev 0 Sequencer
1016.1	Prophet-10 with Rev 1 Sequencer