Sequential Circuits, Inc.
3051 North First Street
San Jose, CA 95134-2093
(408) 946-5240
TELEX: 364412 INTR 706

Nijverheidsweg 11c
3641 RP Mijdrecht
Netherlands
02979-6211
TELEX: 12721 SQNTL NL

Andrew
Mc. Gowan

PROPHET-T8
PRELIMINARY SERVICE DATA
Manual No. TN1008-0
Issued: August, 1983

PRELIMINARY INFORMATION
All subject to change.

GENERAL

For the following discussion, please refer to the accompanying block diagram and schematics.

The computer contains a Z-80B 8-bit Main processor and a 16-bit Z8002A Final processor, both running at 6 MHz.

The Z-80 Main handles the keyboard and control panel inputs, MIDI, and program and sequence data to constantly update Common RAM with current data in the formats required by the Final. For example some of the knobs act as plus/minus controls. In this case the Main would take the 00-FFH number from the ADC and convert it to a plus/minus two's complement sixteen-bit number with the correct weighting. The Z-80 also latches out switch bits to control the analog switches in the synth.

The Z-8002 Final processor calculates the digital envelopes, LFOs, and generates six final CVs for each of the eight voices (48 total) plus a few miscellaneous CVs. It refers to the Common RAM for data which it processes and sends to a First-In-First-Out (FIFO) buffer from which they are eventually clocked out as control voltages (CVs) to the Sample/Holds.

MAIN SYSTEM

The Main processor system consists of the Z-80 CPU, 2764 8K EPROM, five 6116LP Non-volatile static RAMS and the MIDI UART. The memory decoder enables only one of these devices at a time to use the Data bus. NV RAM can not be enabled if power is off.

The various input drivers and output latches are selected by chip selects (CSO-out, CSI-in) from the I/O decoder. The CSs clock:

a decoder for the LED and switch matrices,
a latch for the LED matrix,
a driver for the switch matrix,
a decoder and driver for the keyboard optics,
a miscellaneous latch for tape output and A-440,
a miscellaneous driver for tape and footswitch input,
a latch for programmed volume which drives two level DACs in the audio output stage,
four latches with synth switch signals,
two latches which address and select the multiplexer chips which channel the control knobs and pressure sensors to the Analog-to-Digital Converter (ADC), the ADC and ADC driver (input).

A 1-kHz interrupt clock is provided to both processors. In the Main, M1 is ORed with -IORQ to get INT ACK which resets INT FF. The INT FF has to be reset when first entering the interrupt state so the processor doesn't keep seeing INTs.

The Z-80 interrupt handling is much more complicated (in software) than the Z-8002, because the Main is doing keyboard scanning, knob conversion, switch scanning, LED output, MIDI processing. Keyboard scanning is most critical. It must be done on a 1 millisecond (= 1 kHz) basis to give sufficient resolution for velocity. The Main processor scans the entire keyboard every interrupt cycle. To prevent flickering, the LEDs are also strobed each cycle. Other tasks are accomplished on successive interrupt cycles. The knobs are read in background mode (in the time between the end of the interrupt handler and the appearance of the next INT).

Writing to the low-power RAMS (except Scratchpad) is enabled by a bit from the miscellaneous latch. The signal encounters an RC delay then enables writing (-WR) through an OR-gate. This hardware protects the memories against power-down problems.

FINAL SYSTEM

The Final processor system consists of the Z-8002, two 2732 EPROMS (4K words), the 8253-5 Timer/Counter for Tune and A-440, and the 64-word deep FIFO which is decoded as a single memory location. The Tune control latch is also memory-mapped. The Final Address bus is latched off of the Final Address/Data Bus by a latch driven by AS.

The Z-8002 clears its interrupt with a signal from the status decoder. It only processes every third INT (3 ms). (This gives the envelopes 3 ms. resolution.) Each time it undertakes the same routine for CV calculation. In its spare time (background mode) it processes key on/off information which has been received from the Main.

At the beginning of each interrupt cycle, the Final does a high-speed block move of 59 words to the FIFO. Output Ready (OR) goes high. The processor continues with other tasks while the hardware synchronizes FIFO output to the 14-bit DAC and CV Demultiplexer. The most significant bit of the first word in the FIFO is set, which becomes the S/H CLR signal. This resets the dual 4-bit counter which generates the S/H demultiplexer addresses. Clocked at 62.5 kHz, the counter increments and writes Vdac to each S/H until the FIFO is empty as indicated by OR low.

COMMON RAM AND ARBITRATION

The Main and Final Data busses interface Common RAM through transceivers which are governed ultimately by the Arbitration logic. The Main or Final Address busses define Common RAM locations through an Address bus multiplexer (selector) which is controlled by Z-80 and Z-8002 requests.

Optimized toward the Final processor, Common RAM is sixteen bits wide. The Z-80 can only access one byte at a time of course, so its Common RAM logic is a little more extensive than the Z-8002's because upper or lower bytes have to be selected.

For the Arbitration logic, both processors have REQUEST signals which are decoded memory addresses, ENABLE signals which turn on their Common RAM transceivers, and WAIT signals which tell them to pause. The Final has priority. Actually, neither processor enters a wait state unless there is contention for Common RAM. If both processors request RAM simultaneously, the Main must wait.

SCALING PROCEDURE

Scaling is required periodically, and after any power supply repairs.

1. Allow the unit to warm-up for at least 1/2 hour.

2. Center MASTER TUNE.

3. Center the PITCH wheel.

4. Lower the MOD wheel fully off.

5. Hold RECORD and press PROGRAM/SEQUENCE SELECT #3. This calibrates the wheels.

6. Open the top. Do not unmount any PC boards.

7. Hold A-440 and press TUNE. This activates the computer scaling routine. The routine proceeds by scaling OSC 1A, 1B, and FILT 1, OSC 2A, 2B ...through FILTER 8.

8. Observe the SAVE TO TAPE LED, which may either be lit or unlit. Trim OSC 1A scale trimmer to the point where the LED toggles on and off. There is some hysteresis in the trim--just get it as close as you can.

9. To advance to the next adjustment, press TUNE. In this case this brings up OSC 1B.

10. Advance to the FILT 1 and remaining trims by again pressing TUNE. If you lose track of what trim is appropriate, you can identify active oscillators by probing their pin 8 with a scope, which should show a sawtooth wave. Tuning filters can be identified by a sine wave on their pin 17.

11. After FILTER 8 has been trimmed, the Prophet-T8 will return to normal mode, with the A-440 signal providing audible indication of the end of the procedure.

12. It may be necessary to press TUNE several times to get the instrument into proper tune.

2-XX TUNE

Another feature of analog/digital technology is represented by the T-8 in the tune system. The accuracy of instrument performance is dependant upon the tune system's reliability to keep all sixteen oscillators and eight filters corrected constantly.

Tune occurs in two parts. At power-up, the system accurately measures both oscillator and filter frequencies (In a consecutive order from voice 1 to voice 8) through a nine octave range,and correlates the precise CVs necessary to create perfectly tuned octaves. The system uses a technique called sucessive approximation. In sucessive approximation, the recorded count of the analog pulse is compared to a reference count represented first by the DAC MSB. The computer sets the MSB as long as the pitch does not exceed the reference. This procedure is repeated, setting all fourteen DAC bits in order of the MSB to the LSB. The difference between the actual(14-bit,651uV) and hypothetical (83mV-step) CVs is called tuning "biases". The second part of tuning is active while playing, because the individual bias for the oscillators and filters are recalculated for each keystroke by the computer, and is then corrected for the note that is designated.

Like the Prophet 600, there is no tune multiplexer. Initially, U348-15 TUNE SELECT(TUNE SEL) controls U506 4053 analog switch,which selectively routes AUDIO LEFT(AUDIO L) for voices 1-4 and AUDIO RIGHT(AUDIO R) for voices 5-8 to the TUNE COMPARATOR(TUNE CPR). The computer then selects in order the oscillators and filters which drive U505 TUNE CPR(refer sheet J). TUNE CPR converts OSC and FILT references into pulses. R515 is placed in the feedback loop to prevent oscillations. U345-15 ENABLE TUNE (EN TUNE) acts as a pull-up reference at U505-7 output. The output is sent back to PCB-3 for counting in the tune circuit(refer sheet D).

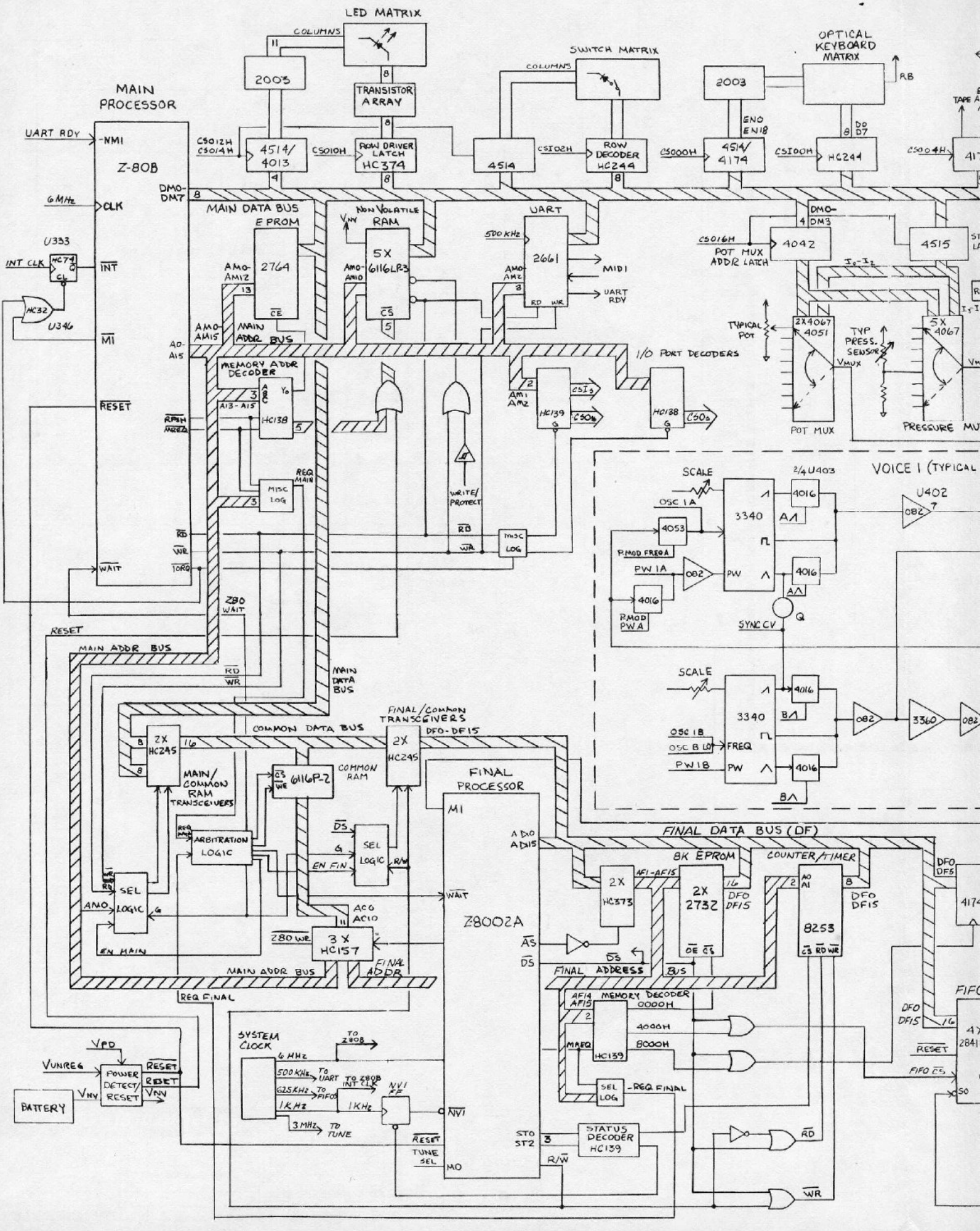
The squared-up OSC/FILT pulses are attenuated through R316 and into U347-12 AND GATE. The computer generates a pulse from U345-2 to U347-13. This pulse serves as a "fake clock" which initializes the one-shot counter of U349 8253-5 Programmable Interval Timer. The PIT includes three independent 16-bit presettable down counters. CNTR 0 is programmed to count one oscillator pulse, but needs the fake clock to begin the count.

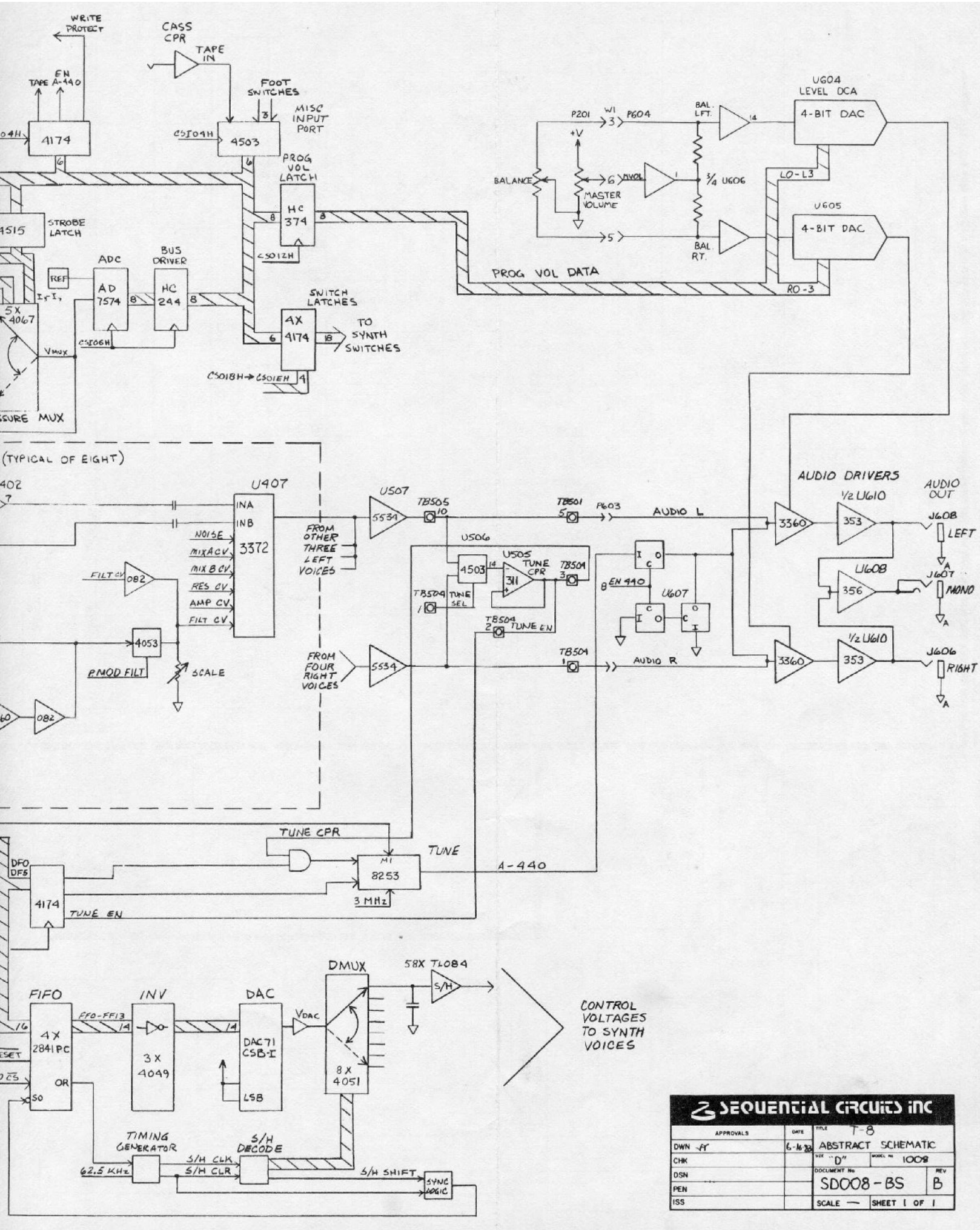
U345-5 latches the gate (G) signal to U349-11, which enables the cycle counter. Then it outputs the fake clock pulse to gate U347-11 high to begin the single count. When the cycle counter recieves the first falling edge, the output (pin 10) goes low. Pin 10 is also connected to MULTI MICRO IN (MI) of U348-7 microprocessor. This monitors the state of the one-shot so thatthe computer knows when to read the total time counter (CNTR 1). The output of CNTR 0 is then inverted, gating on CNTR 1, which will count at a 3MHZ rate. Because CNTR 0 is programmed for a single count, at the next falling edge pin 10 goes high, stopping CNTR 1. CNTR 1 is used to count the amount of 3 MHZ cycles during the analog represented pulse, which is then read through the DATA BUS. The difference between this number of cycles and the given reference causes the CPU to conform S/H CV and sample the given control.

In tuning an oscillator from octave C3 to C4, the reference count is halved because one cycle at C4 approximates half the 3MHZ clock cycles at C3. The reference count

remains the same at octaves C5 - C9, as CNTR 0 doubles its cycle count (2,4,.... ....32). Because of the amount of time it would take to count pulses for C0 - C2 at the low octaves, this information is extrapolated from the curve described by C3 - C9 located in the bias table.

A-440 is activated from U319-5 ENABLE 440 (EN 440) to CNTR 2, U349-16. CNTR 2 divides 3MHZ by 6818 to produce the 440-Hz square wave. EN 440 connects from P301-8 to P602-8 as control for 3/4 U607. When EN 440 is low, output 11 is disabled blocking any signal from CNTR 1. At this time output 9 is also disabled, allowing control pin 5 to be pulled high by R630, enabling this section which grounds out any leakage from pin 11. When EN 440 goes high, pin 6 goes high causing both pin 9 and control pin 5 to be grounded, which causes pin 3 to "float". At the same time control pin 12 is high, allowing the 440 Hz signal to pass at pin 11. A-440 is then inputted at AUDIO L and R at U609-6,9 (refer sheet M).


LED MATRIX
COLUMNS
2003
TRANSISTOR ARRAY
SWITCH MATRIX
COLUMNS
OPTICAL KEYBOARD MATRIX
RB
MAIN PROCESSOR
Z-80B
UART RDY
-NMI
6 MHz
CLK
U333
INT CLK
HC74
INT
HC32
U346
MI
RESET
WAIT
CS012H
CS014H
4514/ 4013
CS010H
ROW DRIVER LATCH HC374
4514
CS102H
ROW DECODER HC244
CS000H
4514/ 4174
CS100H
HC244
CS004H
DMO-DM7
MAIN DATA BUS
EPROM
2764
NON VOLATILE RAM
5X 6116LP-3
UART
500 KHz
2661
MIDI
UART RDY
RD WR
CS016H
POT MUX ADDR LATCH
4042
4515
DMO-DM3
TYPICAL POT
2X4067 4051
TYP PRESS. SENSOR
5X 4067
POT MUX
PRESSURE MU
AMO-AMIS
MAIN ADDR BUS
AO-AIS
MEMORY ADDR DECODER
HC138
A13-A15
I/O PORT DECODERS
HC139
HC138
CS1s
CS0s
WRITE/ PROTECT
MISC LOG
REQ MAIN
RD
WR
IORQ
Z80 WAIT
VOICE 1 (TYPICAL
SCALE
OSC 1A
3340
2/4 U403
4016
U402
4053
P.MOD FREQ A
PW 1A
P.MOD PW A
SYNC CV
SCALE
OSC 1B
OSC B LO
FREQ
PW 1B
3360
COMMON DATA BUS
FINAL/COMMON TRANSCEIVERS
DFO-DF15
2X HC245
MAIN/ COMMON RAM TRANSCEIVERS
6116P-2
COMMON RAM
FINAL PROCESSOR
Z8002A
ARBITRATION LOGIC
SEL LOGIC
EN FIN
EN MAIN
3 X HC157
FINAL ADDR
FINAL DATA BUS (DF)
8K EPROM
2X 2732
COUNTER/TIMER
8253
2X HC373
FINAL ADDRESS BUS
MEMORY DECODER
0000H
4000H
8000H
HC139
MAEQ
SEL LOG
REQ FINAL
STATUS DECODER HC139
ST0 ST2
R/W
RD
WR
SYSTEM CLOCK
6 MHz
500 KHz
TO UART
625 KHz
TO FIFOS
1K Hz
3 MHz
TO TUNE
TO Z80B
INT CLK
NVI FF
NVI
RESET
TUNE SEL
MO
VPD
VUNREG
VNV
POWER DETECT/ RESET
BATTERY
FIFO
FIFO CS
SO



SEQUENTIAL CIRCUITS INC

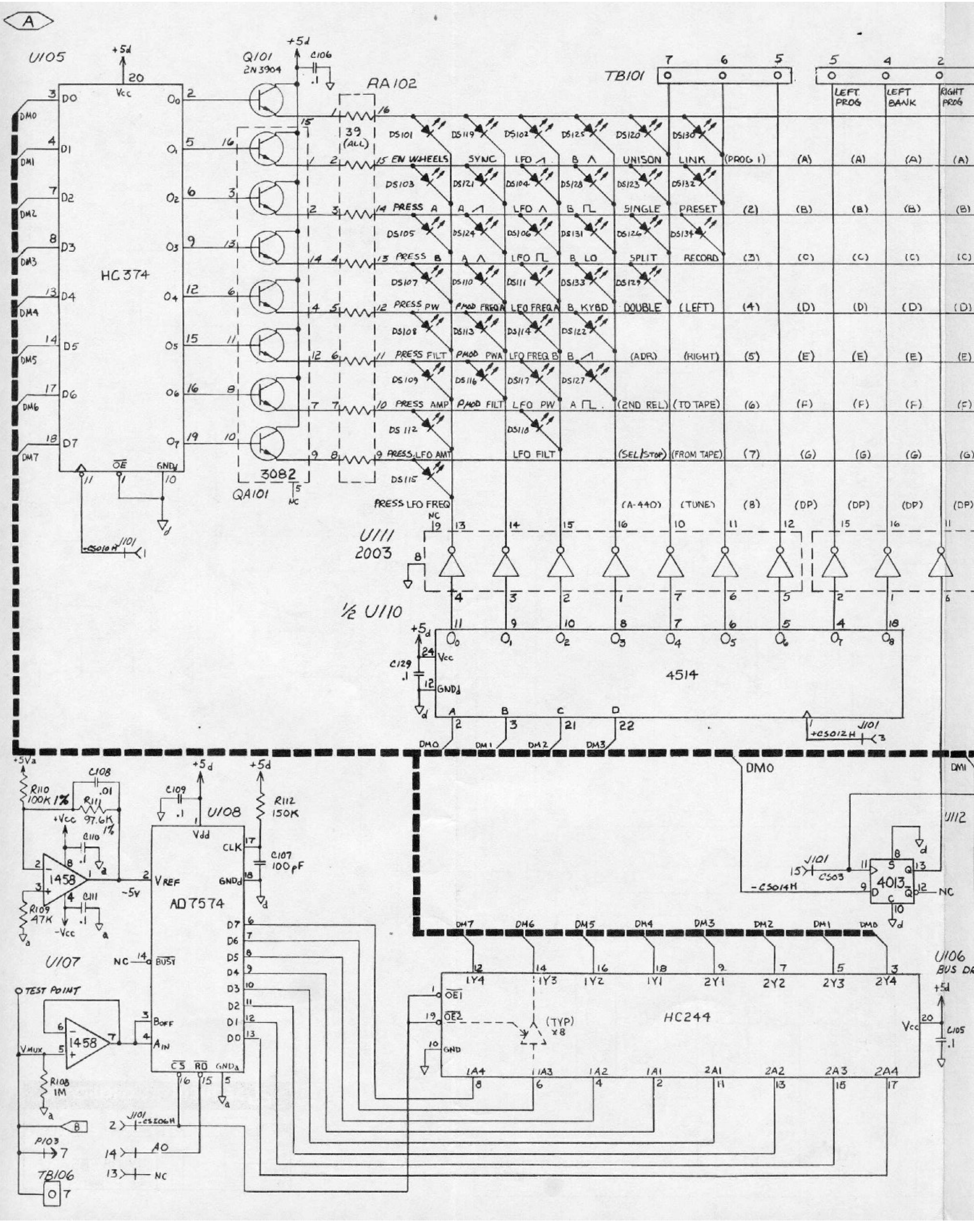
APPROVALS	DATE
DWN AT	6-16-82
CHK	
DSN	
PEN	
ISS	

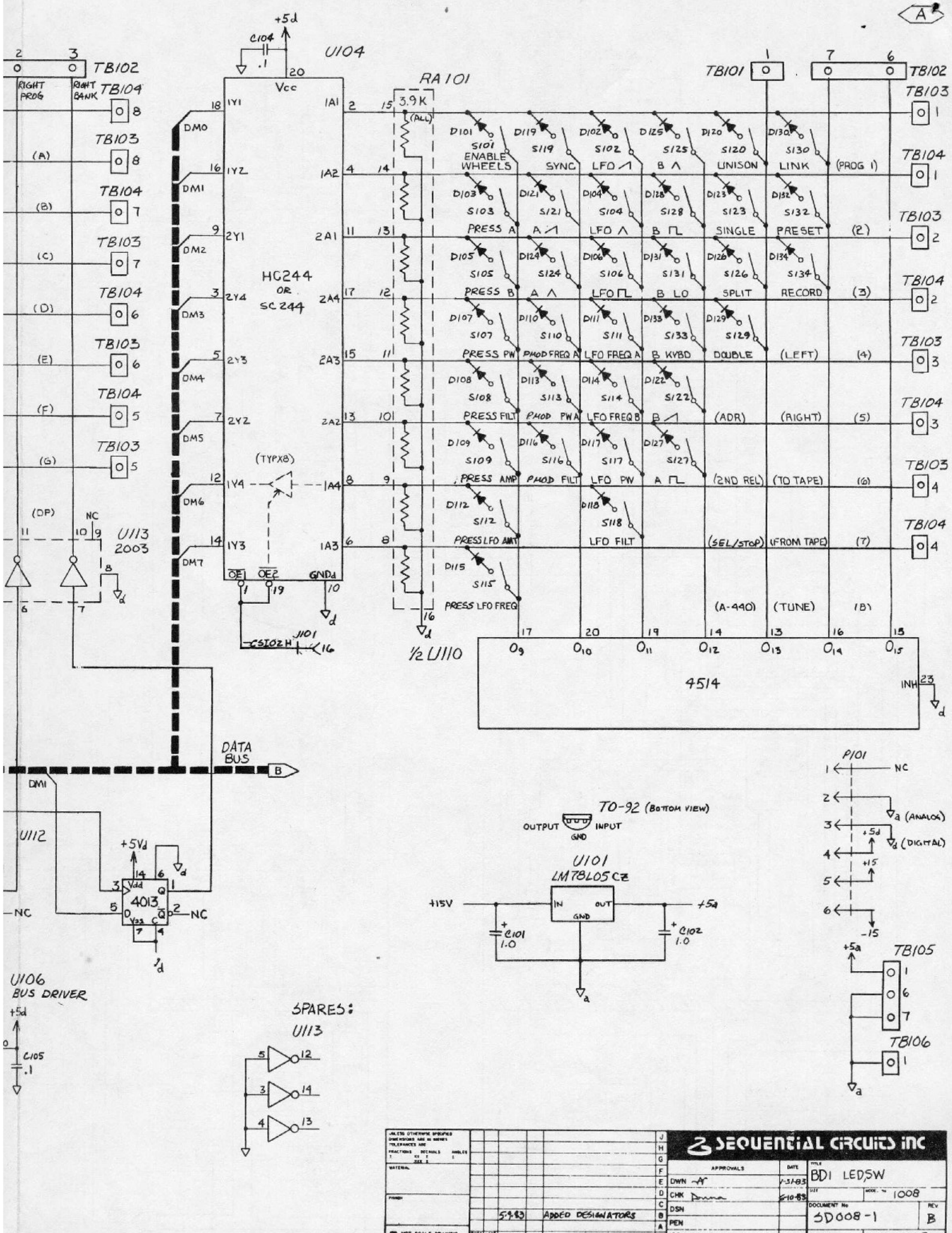
TITLE T-8 ABSTRACT SCHEMATIC

SIZE "D" MODEL No 1008

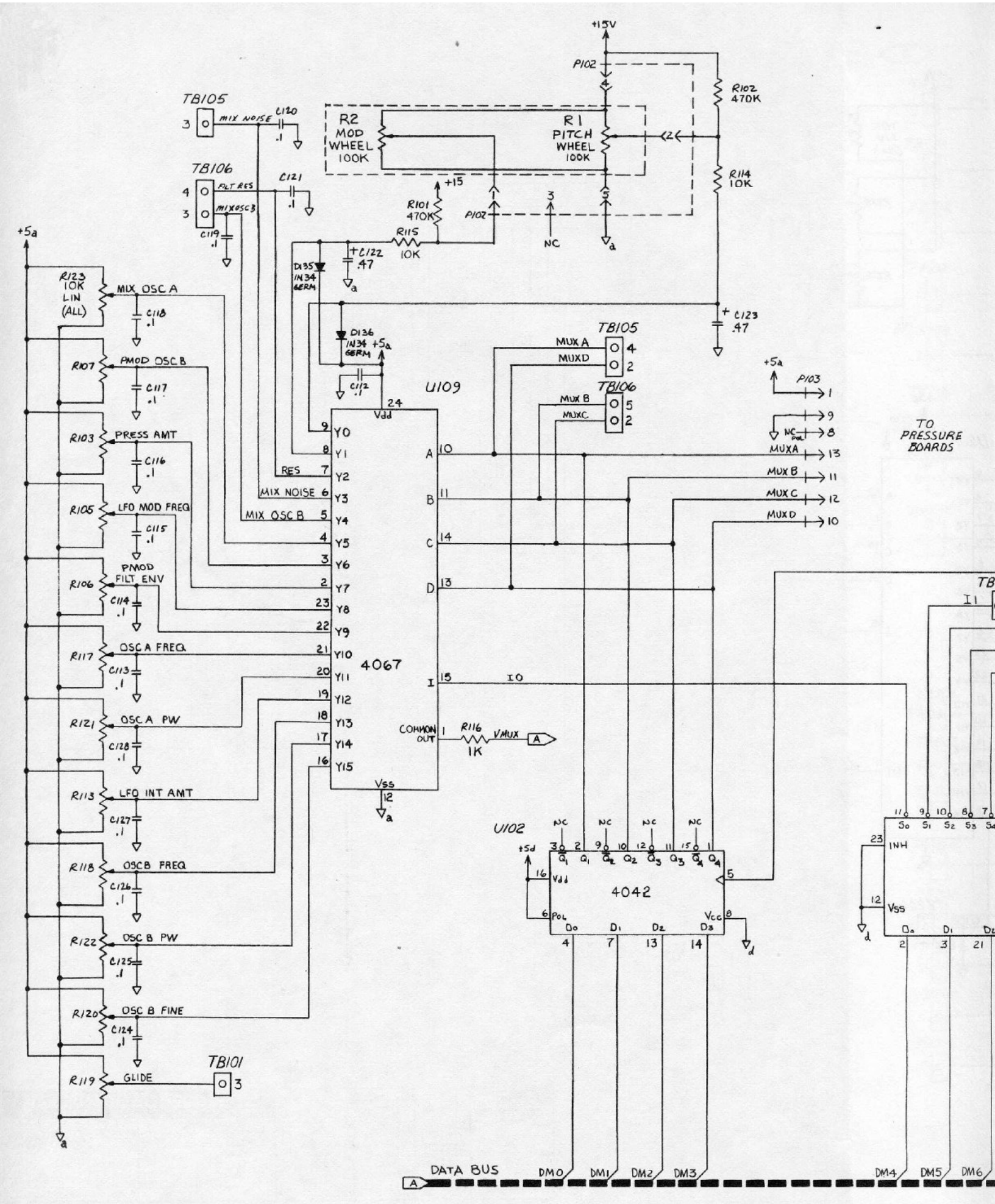
DOCUMENT No SD008-BS REV B

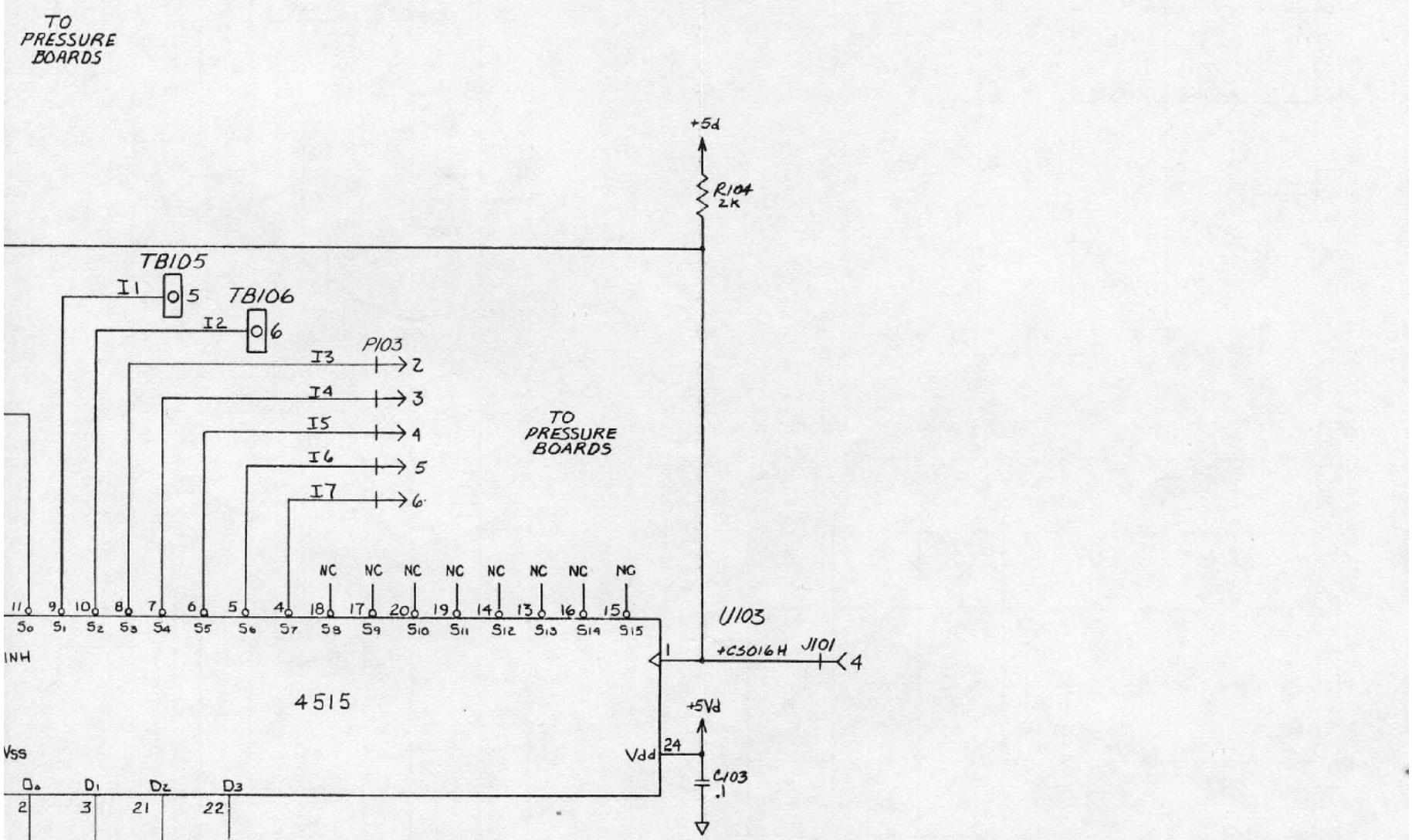
SCALE — SHEET 1 OF 1


A
U105
HC374
+5d
Vcc
GNDd
OE
Q101
2N3904
C106
RA102
39 (ALL)
QA101
3082
TB101
LEFT PROG
LEFT BANK
RIGHT PROG
DS101
DS119
DS102
DS125
DS120
DS130
EN WHEELS
SYNC
LFO
UNISON
LINK
(PROG 1)
PRESS A
SINGLE
PRESET
PRESS B
LFO
B LO
SPLIT
RECORD
PRESS PW
PMOD FREQA
LFO FREQA
B KYBD
DOUBLE
(LEFT)
PRESS FILT
PMOD PWA
LFO FREQ B
(ADR)
(RIGHT)
PRESS AMP
PMOD FILT
LFO PW
(2ND REL)
(TO TAPE)
PRESS LFO AMT
LFO FILT
(SEL/STOP)
(FROM TAPE)
PRESS LFO FREQ
(A-440)
(TUNE)
(DP)
U111
2003
1/2 U110
4514
C129
J101
+CS012H
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
+5Va
R110
100K 1%
C108
R111
97.6K 1%
+Vcc
-Vcc
C110
C111
1458
R109
47K
-5v
C109
U108
Vdd
R112
150K
CLK
C107
100pF
VREF
AD7574
BUSY
NC
U107
TEST POINT
VMUX
BOFF
AIN
R108
1M
CS
RD
GNDa
-CS206H
P103
TB106
A0
U112
4013
C503
-CS014H
U106
BUS DR
HC244
(TYP) x8
C105
-CS010H



						SEQUENTIAL CIRCUITS INC	
					APPROVALS	DATE	TITLE: BD1 LED,SW
				E	DWN AF	7-31-83	
				D	CHK Dana	8-10-83	SIZE: B MODEL No: 1008
				C	DSN		DOCUMENT No: 3D008-1 REV: B
			5-9-83	B	PEN	ADDED DESIGNATORS	
DO NOT SCALE DRAWING			DATE	A	ISS	REVISION	SCALE: SHEET 1 OF 2


+15V
P102
R102 470K
R114 10K
R2 MOD WHEEL 100K
R1 PITCH WHEEL 100K
TB105
MIX NOISE
C120 .1
TB106
FILT RES
MIXOSC3
C121 .1
C119 .1
R101 470K
R115 10K
+15
NC
C122 .47
D135 IN34 GERM
D136 IN34 GERM
C123 .47
+5a
R123 10K LIN (ALL)
MIX OSC A
C118 .1
R107
PMOD OSC B
C117 .1
R103
PRESS AMT
C116 .1
R105
LFO MOD FREQ
C115 .1
R106
PMOD FILT ENV
C114 .1
R117
OSC A FREQ
C113 .1
R121
OSC A PW
C128 .1
R113
LFO INT AMT
C127 .1
R118
OSC B FREQ
C126 .1
R122
OSC B PW
C125 .1
R120
OSC B FINE
C124 .1
R119
GLIDE
TB101
U109
4067
Vdd
Vss
RES
MIX NOISE
MIX OSC B
COMMON OUT
R116 1K
VMUX
MUX A
MUX B
MUX C
MUX D
P103
TO PRESSURE BOARDS
U102
4042
INH
Vdd
Vss
Vcc
Pol
DATA BUS
DM0
DM1
DM2
DM3
DM4
DM5
DM6



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES						J
						H
						G
MATERIAL						F
						E
FINISH						D
		5-9-83		ADDED D135,136 + DESIGNATORS	B	C
DO NOT SCALE DRAWING	FIRST LAST S/N	DATE	ECR No	REVISION	LTR	A

SEQUENTIAL CIRCUITS INC

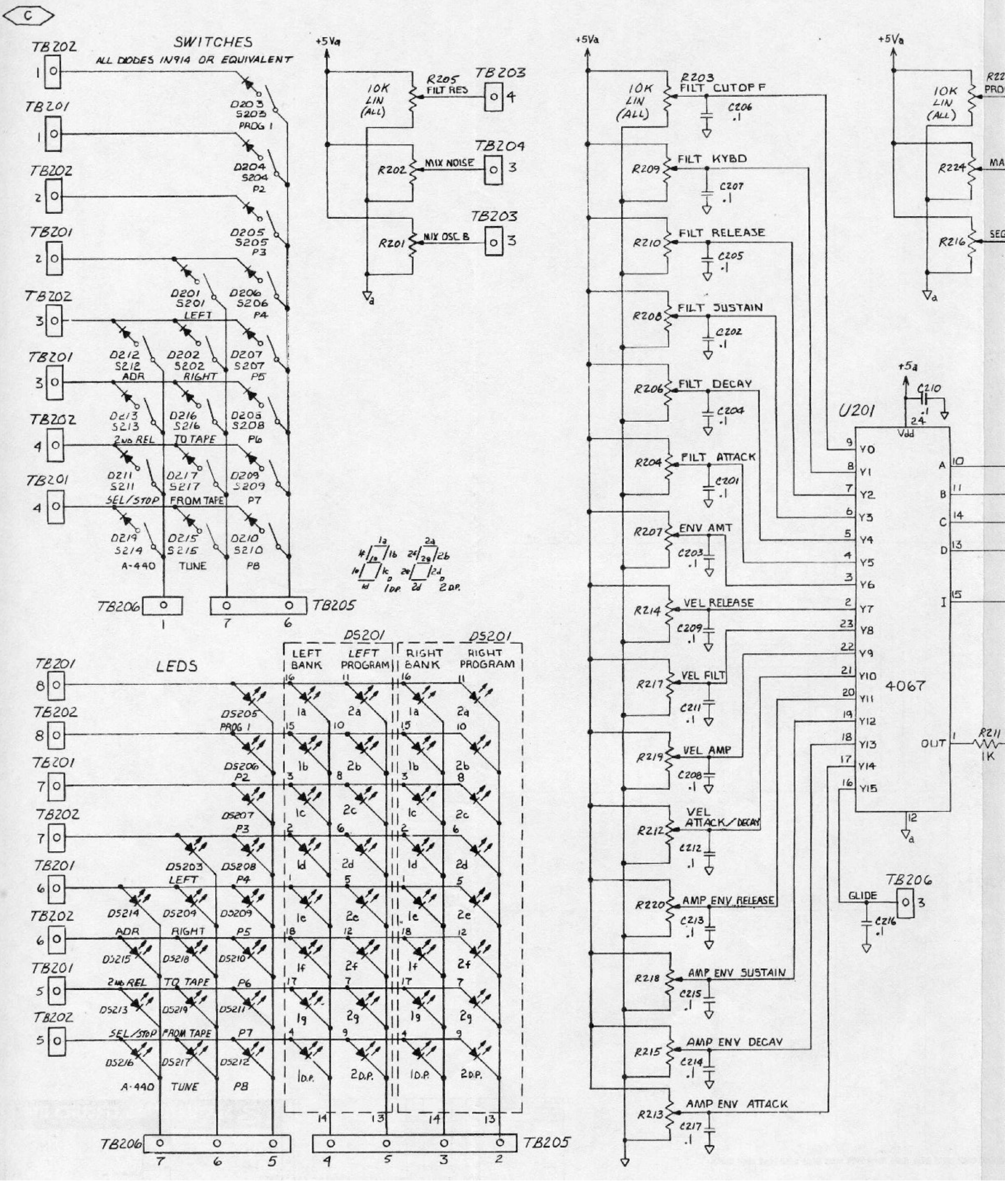
APPROVALS	DATE
DWN AY	1-28-83
CHK Downs	6-10-83
DSN	
PEN	
ISS	

TITLE: LEFT BD1 FRT PANEL

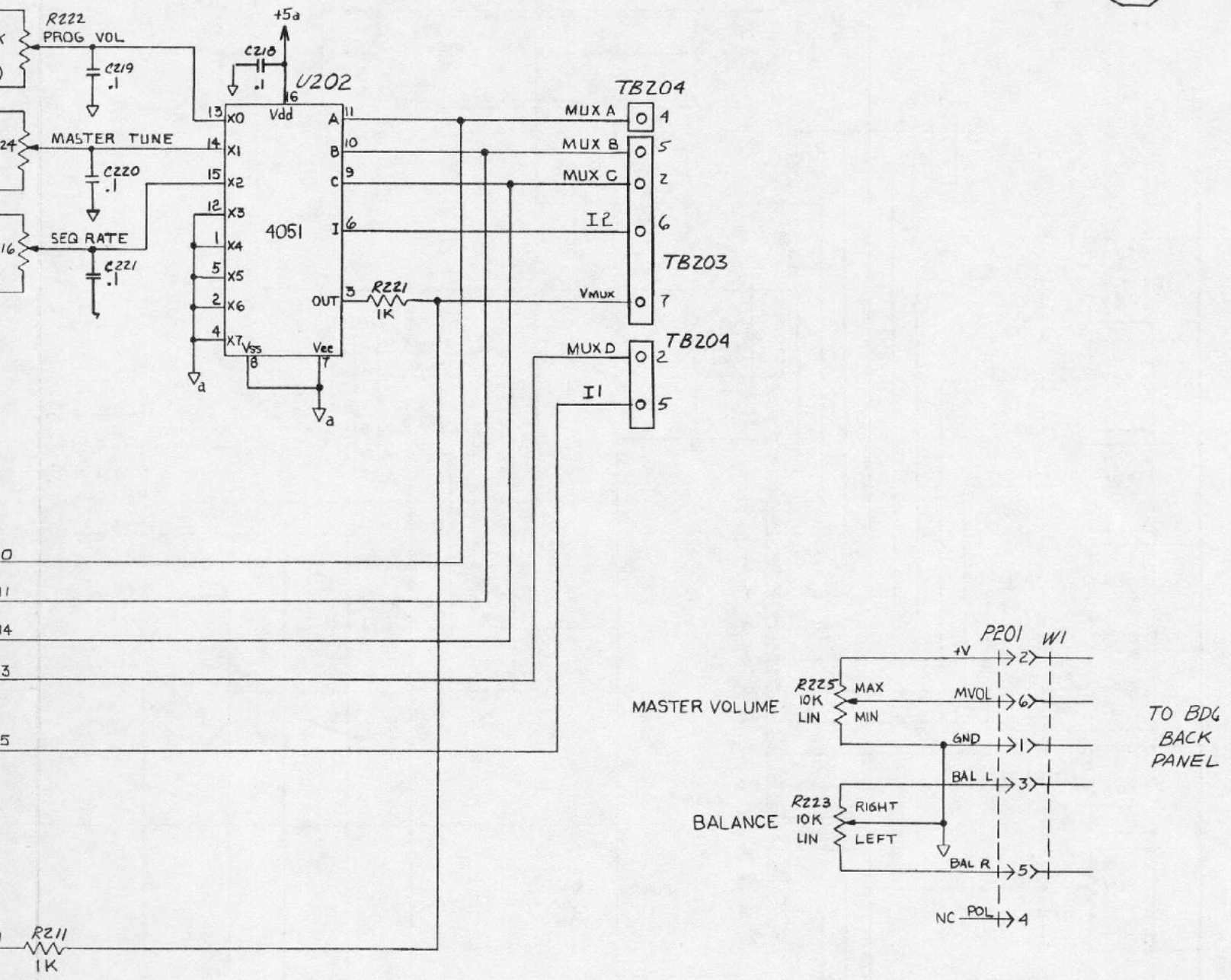
SIZE: | MODEL No. 1008

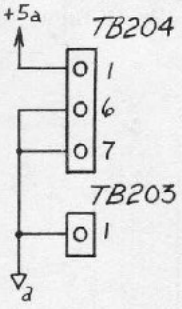
DOCUMENT No. 5D008-1 | REV B

SCALE | SHEET 2 OF 2



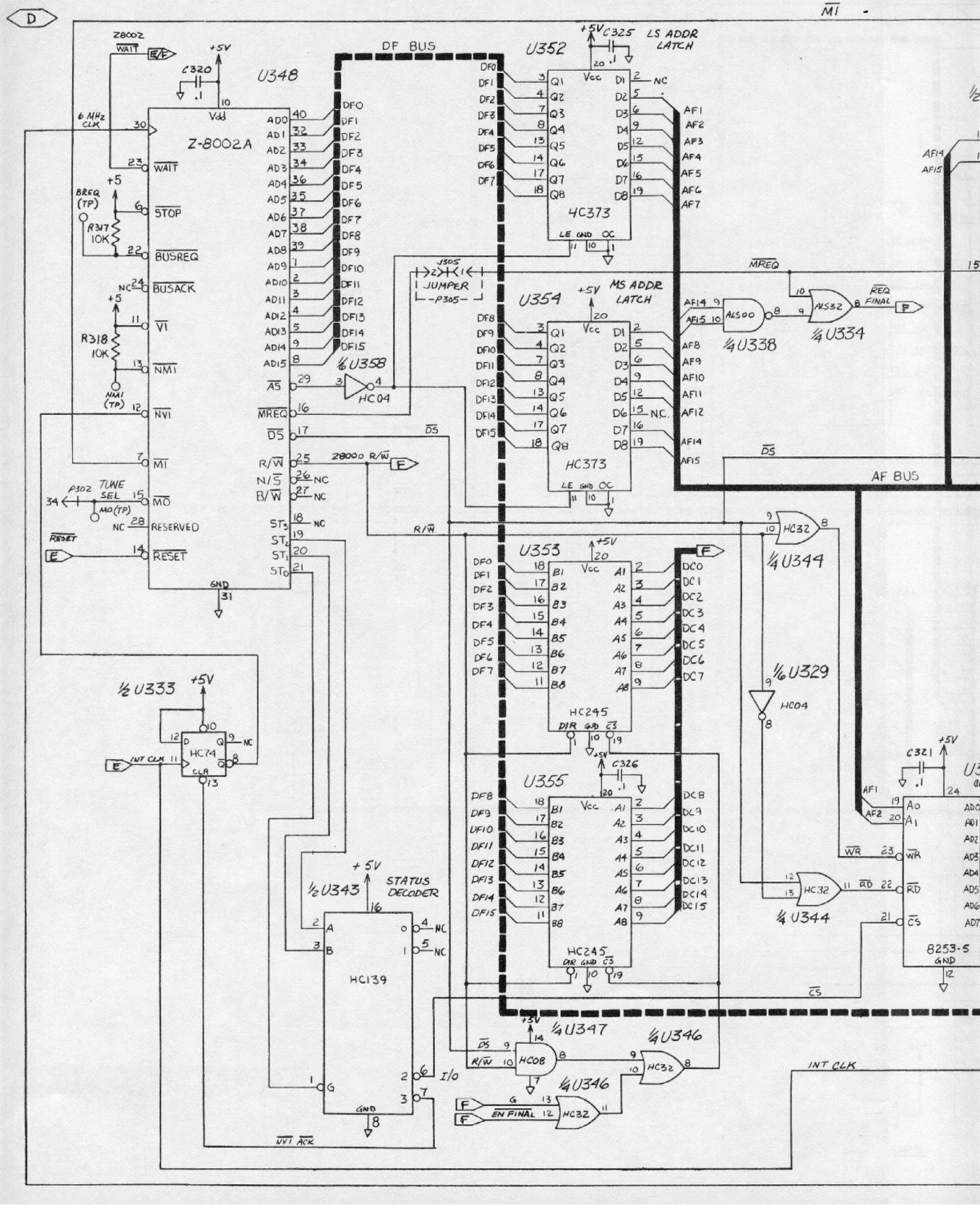
C
SWITCHES
ALL DIODES IN914 OR EQUIVALENT
TB202
TB201
D203 S203 PROG 1
D204 S204 P2
D205 S205 P3
D201 S201 LEFT
D206 S206 P4
D212 S212 ADR
D202 S202 RIGHT
D207 S207 P5
D213 S213 2ND REL
D216 S216 TO TAPE
D208 S208 P6
D211 S211 SEL/STOP
D217 S217 FROM TAPE
D209 S209 P7
D219 S214 A-440
D215 S215 TUNE
D210 S210 P8
TB206
TB205
+5Va
10K LIN (ALL)
R205 FILT RES
TB203
R202 MIX NOISE
TB204
R201 MIX OSC B
LEDS
DS201
LEFT BANK
LEFT PROGRAM
RIGHT BANK
RIGHT PROGRAM
DS205 PROG 1
DS206 P2
DS207 P3
DS203 LEFT
DS208 P4
DS214 ADR
DS204 RIGHT
DS209 P5
DS215 2ND REL
DS218 TO TAPE
DS210 P6
DS213 SEL/STOP
DS219 FROM TAPE
DS211 P7
DS216 A-440
DS217 TUNE
DS212 P8
1D.P.
2D.P.
R203 FILT CUTOFF
C206 .1
R209 FILT KYBD
C207 .1
R210 FILT RELEASE
C205 .1
R208 FILT SUSTAIN
C202 .1
R206 FILT DECAY
C204 .1
R204 FILT ATTACK
C201 .1
R207 ENV AMT
C203 .1
R214 VEL RELEASE
C209 .1
R217 VEL FILT
C211 .1
R219 VEL AMP
C208 .1
R212 VEL ATTACK/DECAY
C212 .1
R220 AMP ENV RELEASE
C213 .1
R218 AMP ENV SUSTAIN
C215 .1
R215 AMP ENV DECAY
C214 .1
R213 AMP ENV ATTACK
C217 .1
U201
4067
Vdd
+5a
C210 .1
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y11 Y12 Y13 Y14 Y15
A B C D I OUT
R211 1K
GLIDE
TB206
C216 .1
R224
R216





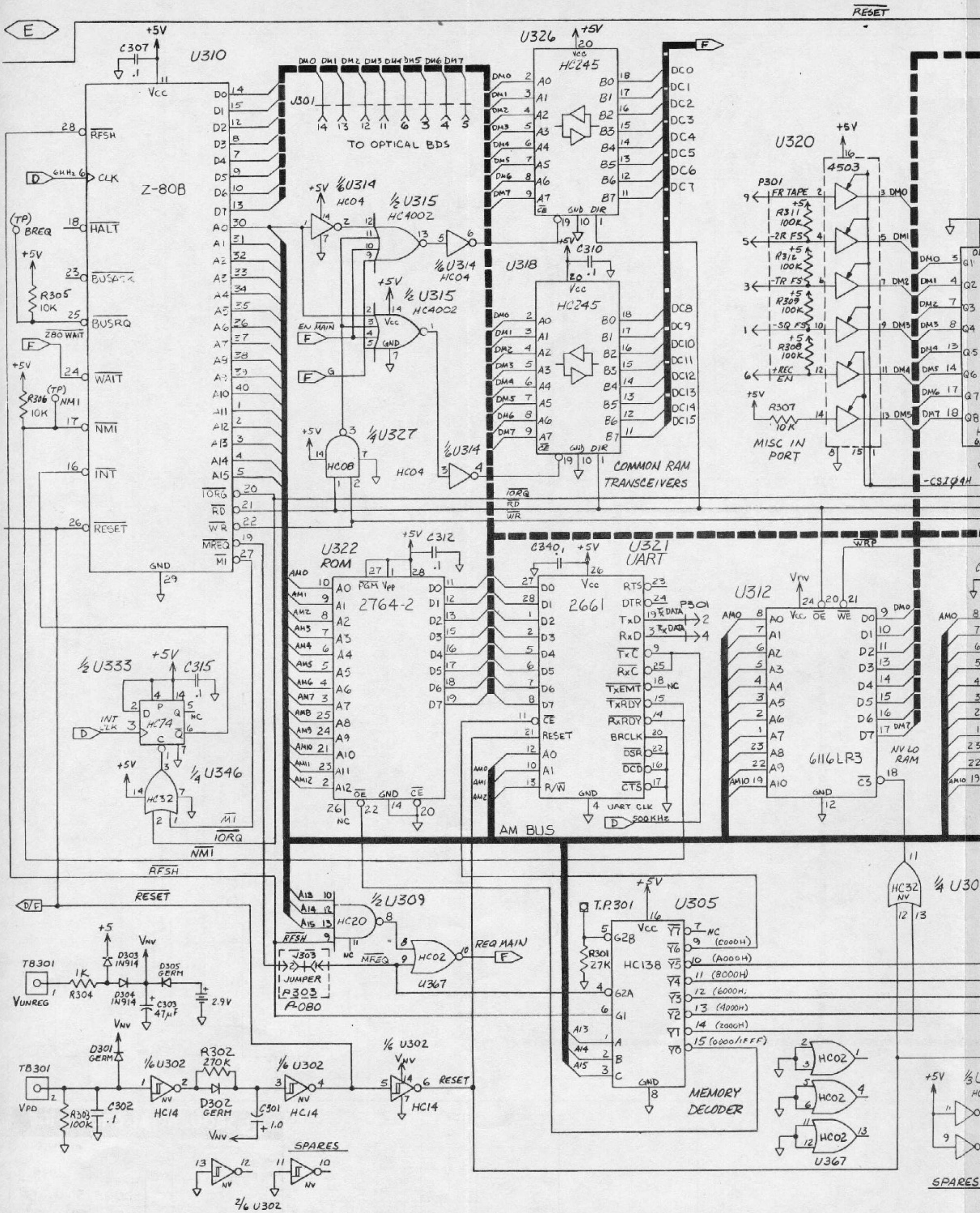
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .X MATERIAL FINISH DO NOT SCALE DRAWING	FIRST/LAST S/N	DATE	ECR No	REVISION	LTR	J H G F E D C B A	SEQUENTIAL CIRCUITS INC	
							APPROVALS	DATE
							DWN A	1-31-83
							CHK Donna	6-9-83
							DSN	
							PEN	
							ISS	

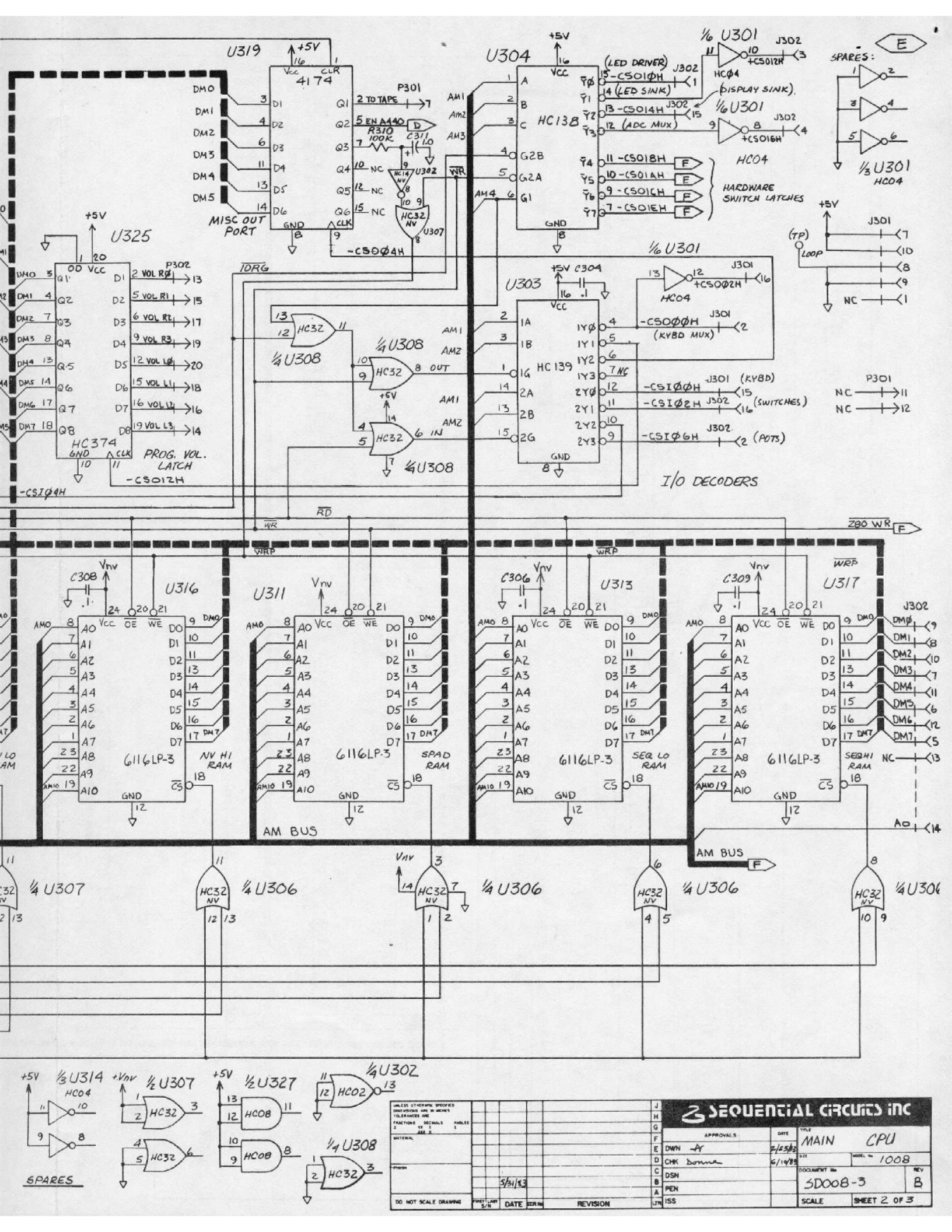
TITLE: PCB2 POT MUX, SW, L.
SIZE: | MODEL No: 1008
DOCUMENT No: SD 008-2-0 | REV: A
SCALE | SHEET 1 OF 1



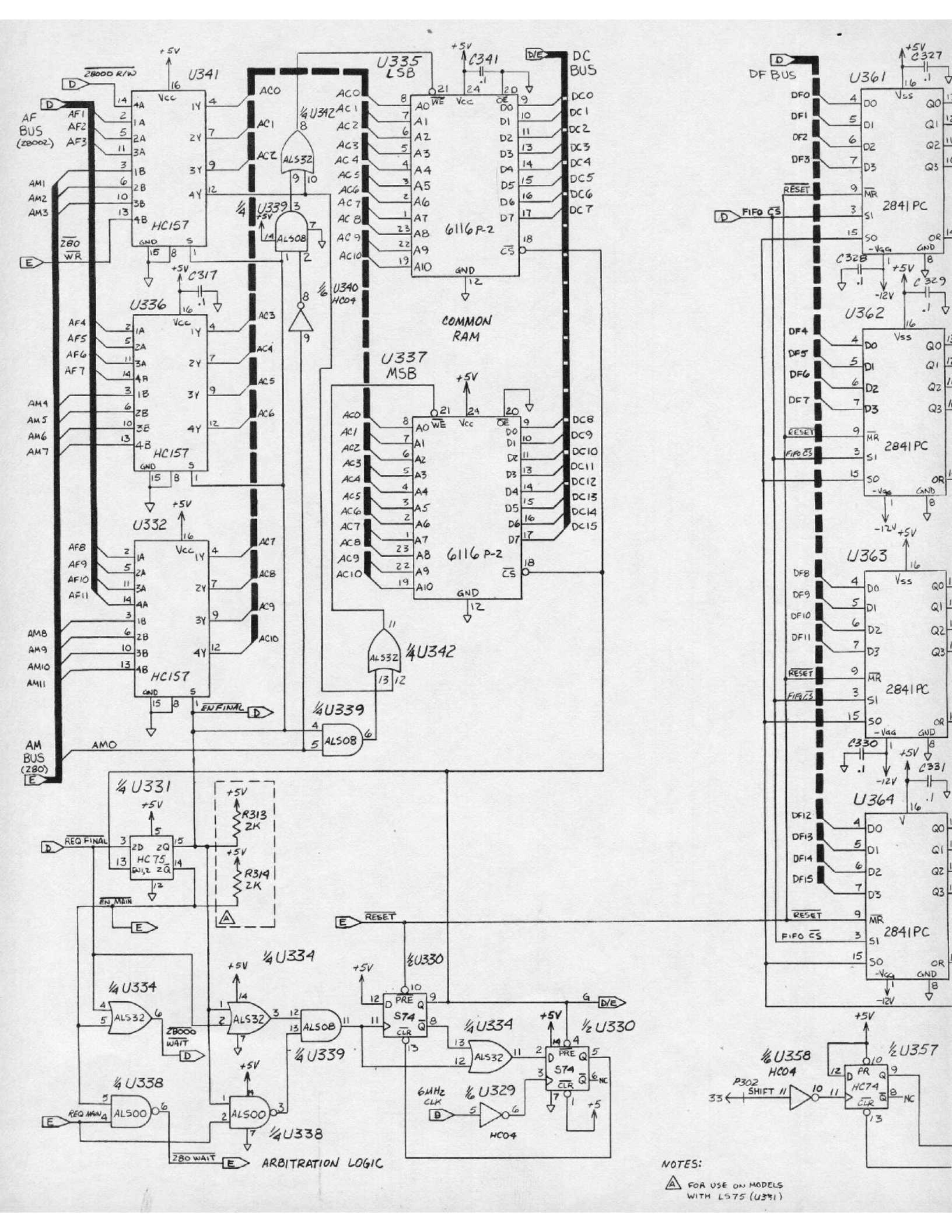
D
Z-8002A
U348
DF BUS
AF BUS
U352
LS ADDR LATCH
U354
MS ADDR LATCH
U353
U355
HC373
HC245
HC139
STATUS DECODER
1/2 U343
1/2 U333
HC74
8253-5
1/6 U358
HC04
1/6 U329
1/4 U338
ALS00
1/4 U334
ALS32
1/4 U344
HC32
1/4 U347
HC08
1/4 U346
JUMPER
J305
P305
Z8000 R/W
REQ FINAL
EN FINAL
INT CLK
NVI ACK
6 MHz CLK
TUNE SEL
P302
MO (TP)
BREQ (TP)
NMI (TP)
R317 10K
R318 10K
C320
C321
C325
C326
WAIT
STOP
BUSREQ
BUSACK
VI
NMI
NVI
MI
MO
RESERVED
RESET
MREQ
DS
R/W
N/S
B/W
CS
RD
WR

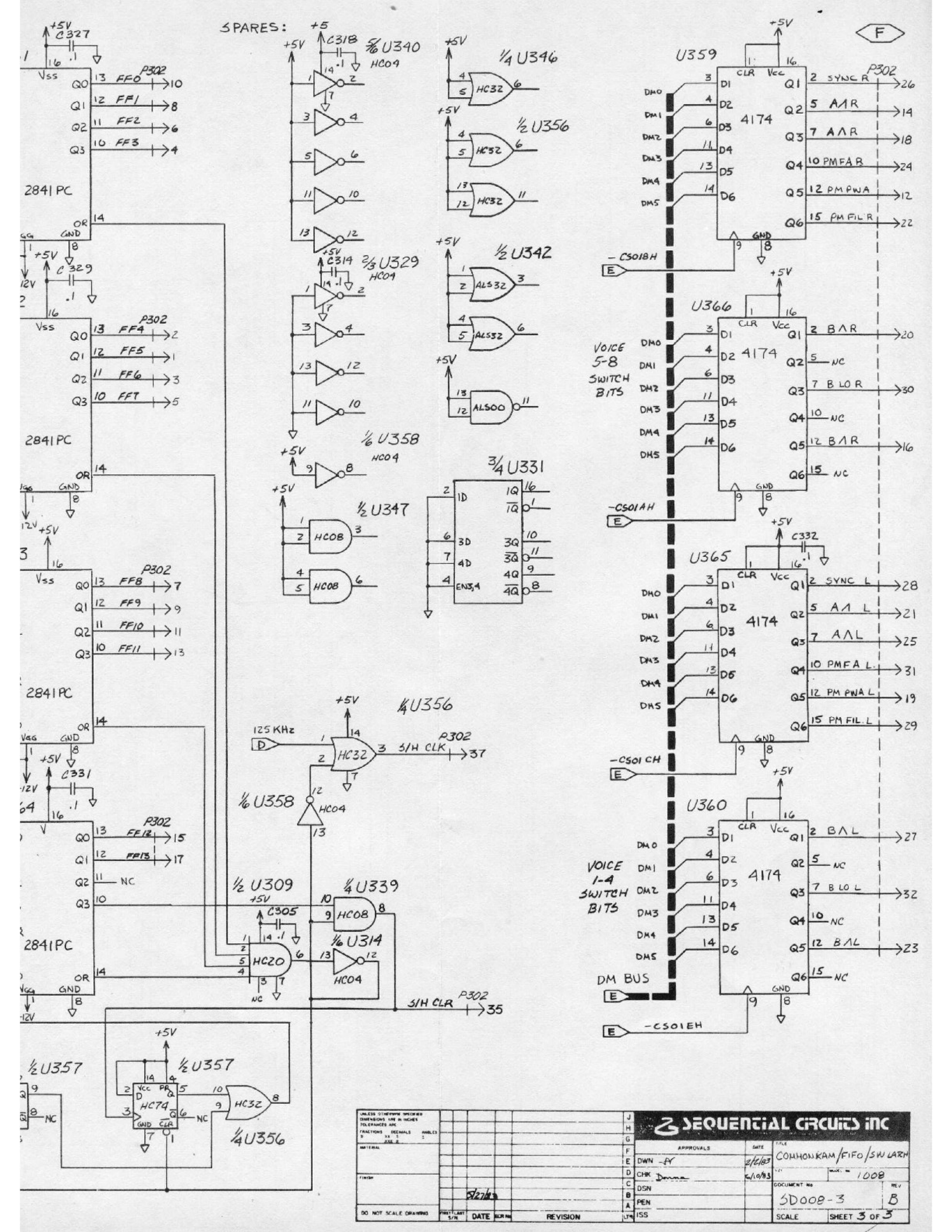
D
U3
MEMORY
DECODER
½U343
HC139
¼U344
HC32
⅙U358
HC04
FIFO C3
F
C324
10pF
R316
10K
TUNE CPR
P302
40
TB301
+5V
-12V
¼U347
HC08
U345
4174
CLR Vdd
GND
EN TUNE
P302
36
⅓U349
8253-5
⅙U358
HC04
G1
G2
A440
EN A440
ENA440
P301
3 MHz
(BACK PANEL)
C3
DS
AF BUS
E
U350
LSB
U351
MSB
C322
C323
2732A
R315
2K
¼U327
UART CLK
500KHz
U349
COUNTER/
TIMER
62.5 KHz
U328
U324
HC393
U323
K1160
C313
6MHz CLK
P304
J304
DF BUS
Z80
CLK
.98KHz
SEQUENTIAL CIRCUITS INC
APPROVALS
DWN
CHK Donna
DSN
PEN
ISS
FINAL
CPU
1008
5D008-3
B
SCALE
SHEET 1 OF 3
DO NOT SCALE DRAWING
REVISION


U310
Z-80B
U326
HC245
U318
COMMON RAM TRANSCEIVERS
U320
4503
MISC IN PORT
TO OPTICAL BDS
U322 ROM
2764-2
U321 UART
2661
U312
6116LR3
NV LO RAM
AM BUS
½ U333
HC74
¼ U346
HC32
½ U309
HC20
U367
HC02
REQ MAIN
U305
HC138
MEMORY DECODER
JUMPER
P303
P-080
TB301
VUNREG
VPD
SPARES
RESET
2/6 U302

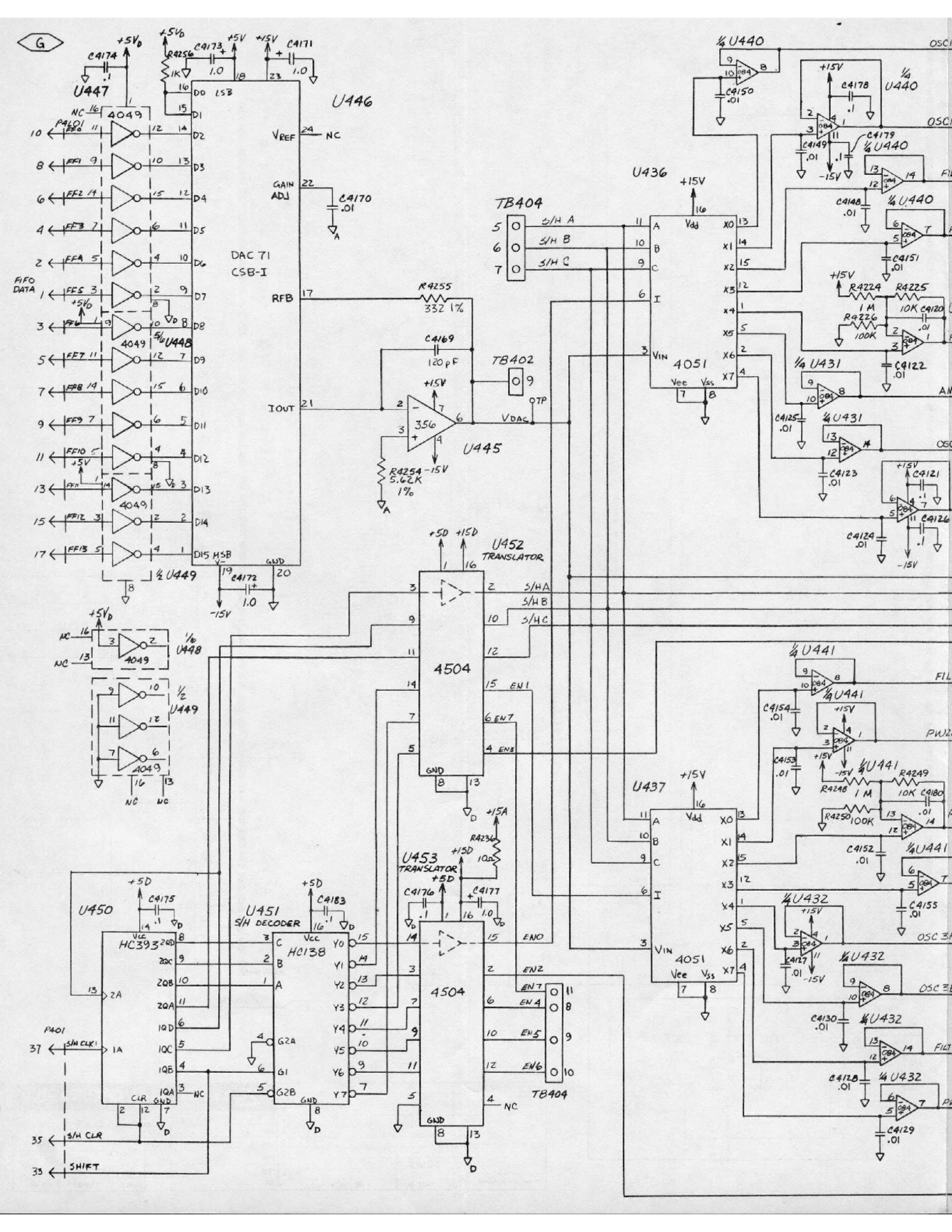


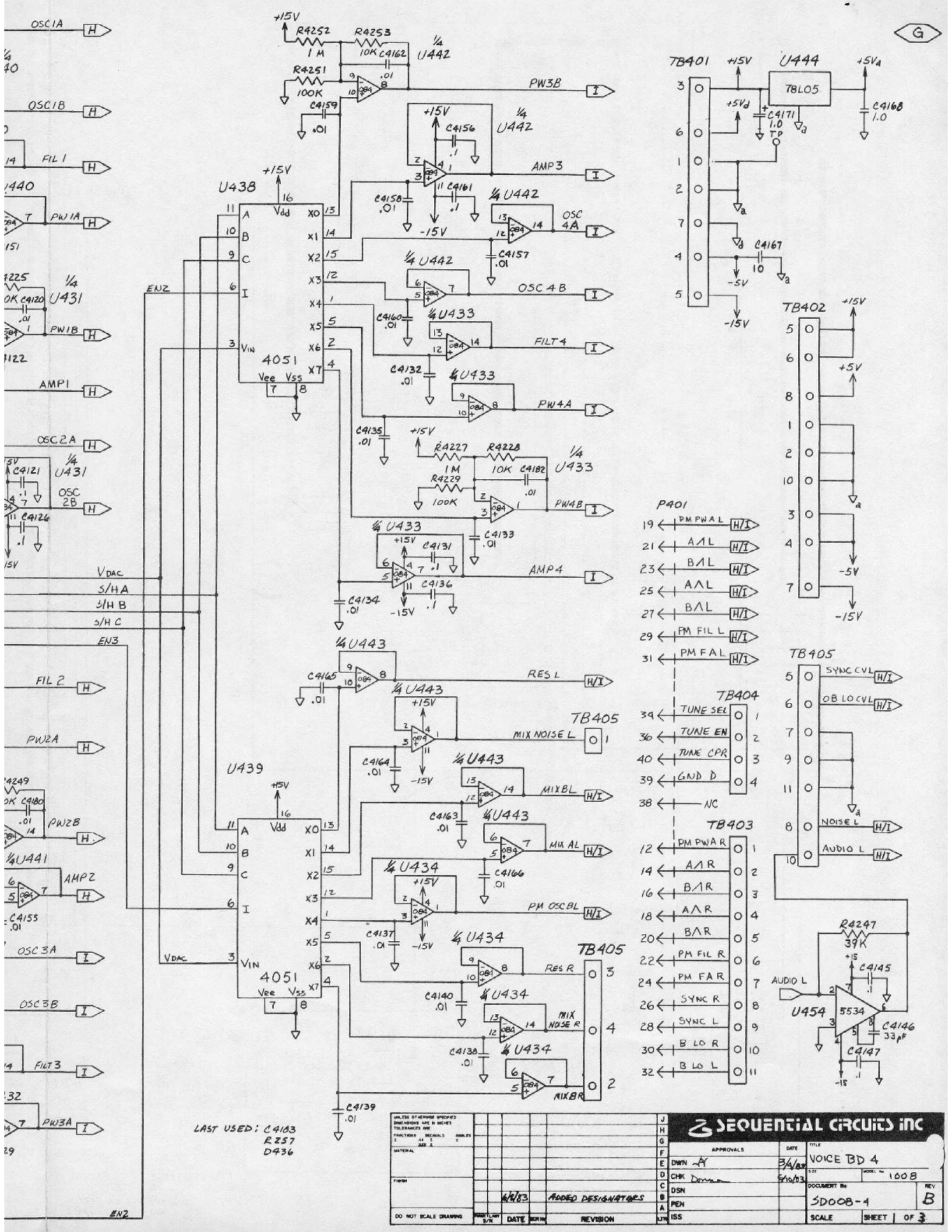
J	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES							SEQUENTIAL CIRCUITS INC		
H										
G										
F								APPROVALS	DATE	TITLE MAIN CPU
E	MATERIAL							DWN AY	2/25/83	
D	FINISH							CHK Donna	6/14/85	SIZE MODEL No 1008
C								DSN		DOCUMENT No 5D008-3 REV B
B								PEN		
A	DO NOT SCALE DRAWING							ISS		SCALE SHEET 2 OF 3
JTR		FIRST USED ON	5/31/83	DATE	ECO No	REVISION				

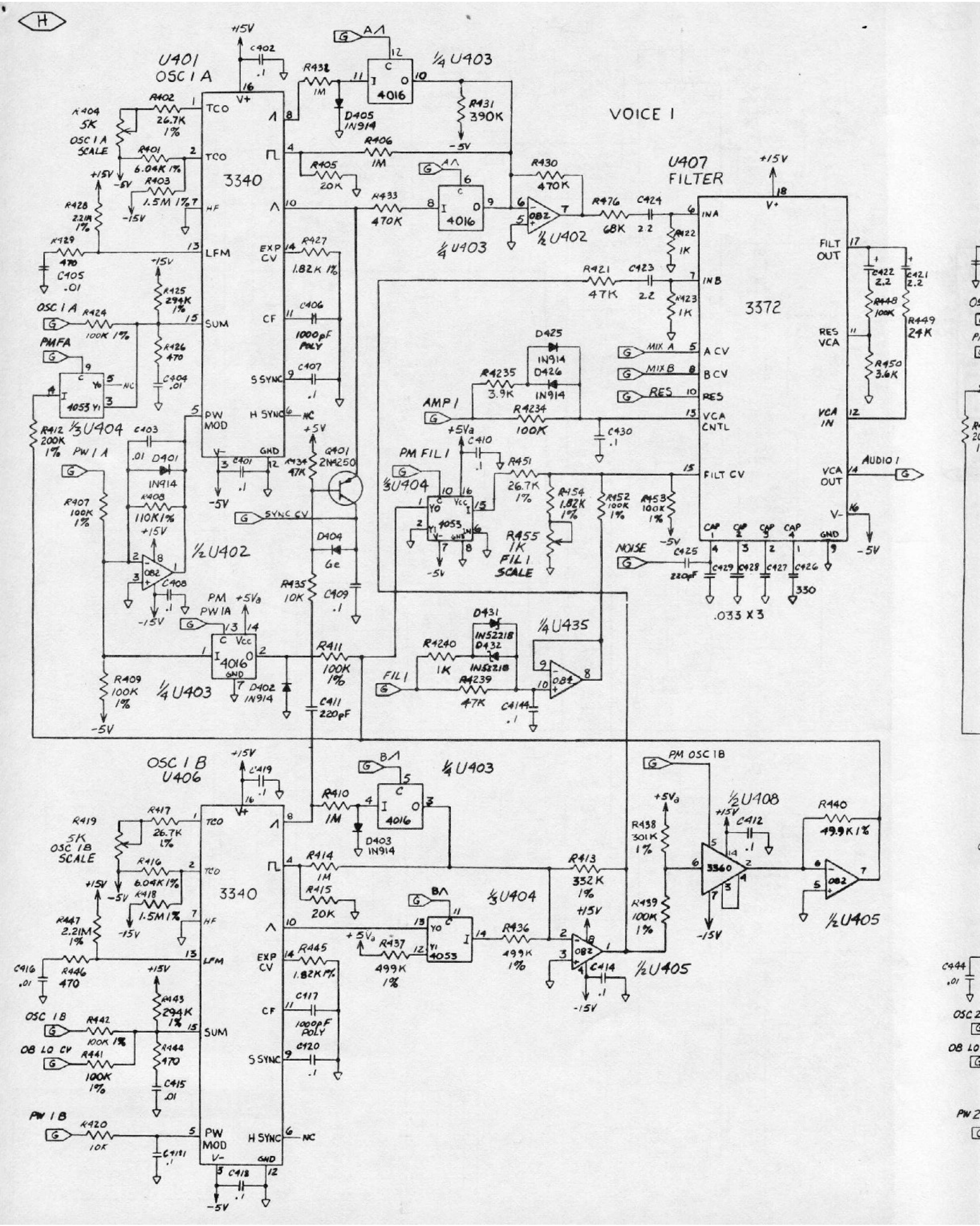

U341
U335 LSB
U336
U332
U337 MSB
U339
U340 HC04
U342
U361
U362
U363
U364
2841PC
6116P-2
HC157
COMMON RAM
DC BUS
DF BUS
AF BUS (Z80D2)
AM BUS (Z80)
Z80D0 R/W
Z80 WR
EN FINAL
AMO
U331
R313 2K
R314 2K
REQ FINAL
EN MAIN
U334
U330
U338
U329
U358 HC04
U357
HC74
S74
HC75
ALS32
ALS08
ALS00
6MHz CLK
SHIFT
P302
REQ MAIN
Z80 WAIT
Z80D0 WAIT
ARBITRATION LOGIC
NOTES:
A FOR USE ON MODELS WITH LS75 (U331)

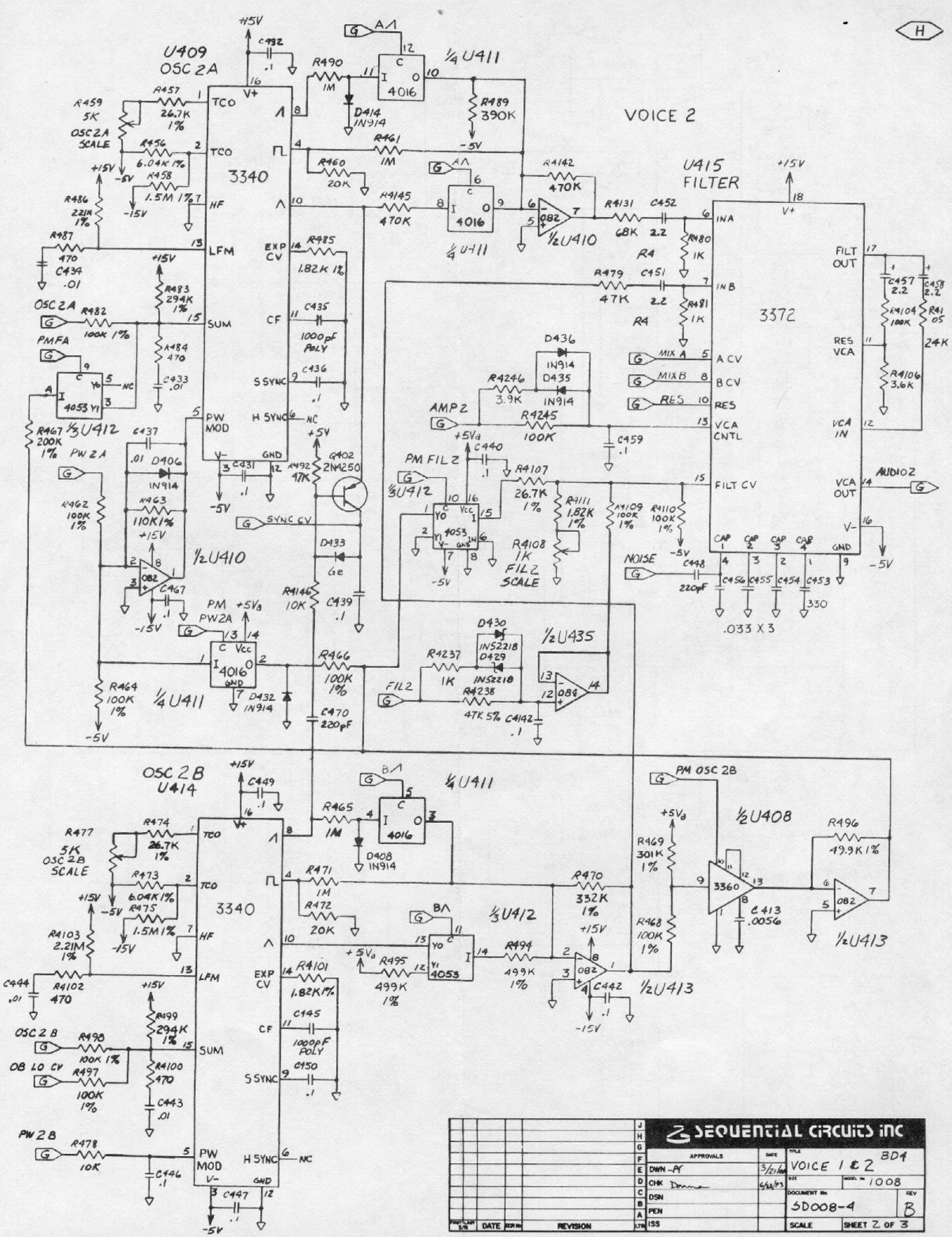


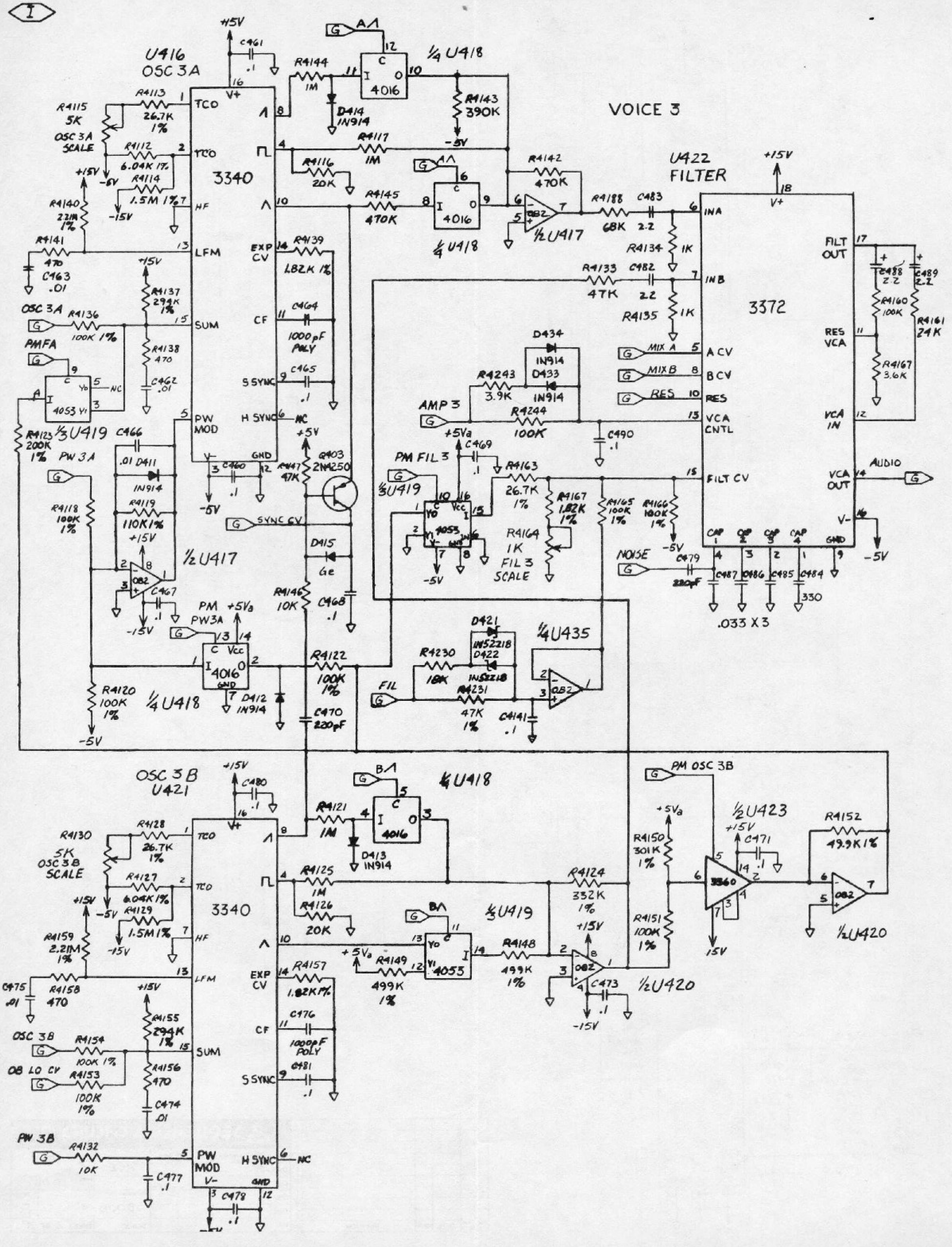
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .X	SEQUENTIAL CIRCUITS INC		
MATERIAL	APPROVALS	DATE	TITLE: COMMON RAM/FIFO/SW LATCH
FINISH	DWN -FF	2/2/83	
	CHK Dana	5/10/83	SIZE: MODEL NO: 1008
DO NOT SCALE DRAWING	DSN		DOCUMENT NO: SD008-3 REV: B
	PEN		
	ISS		SCALE: SHEET 3 OF 3
	DATE REVISION		

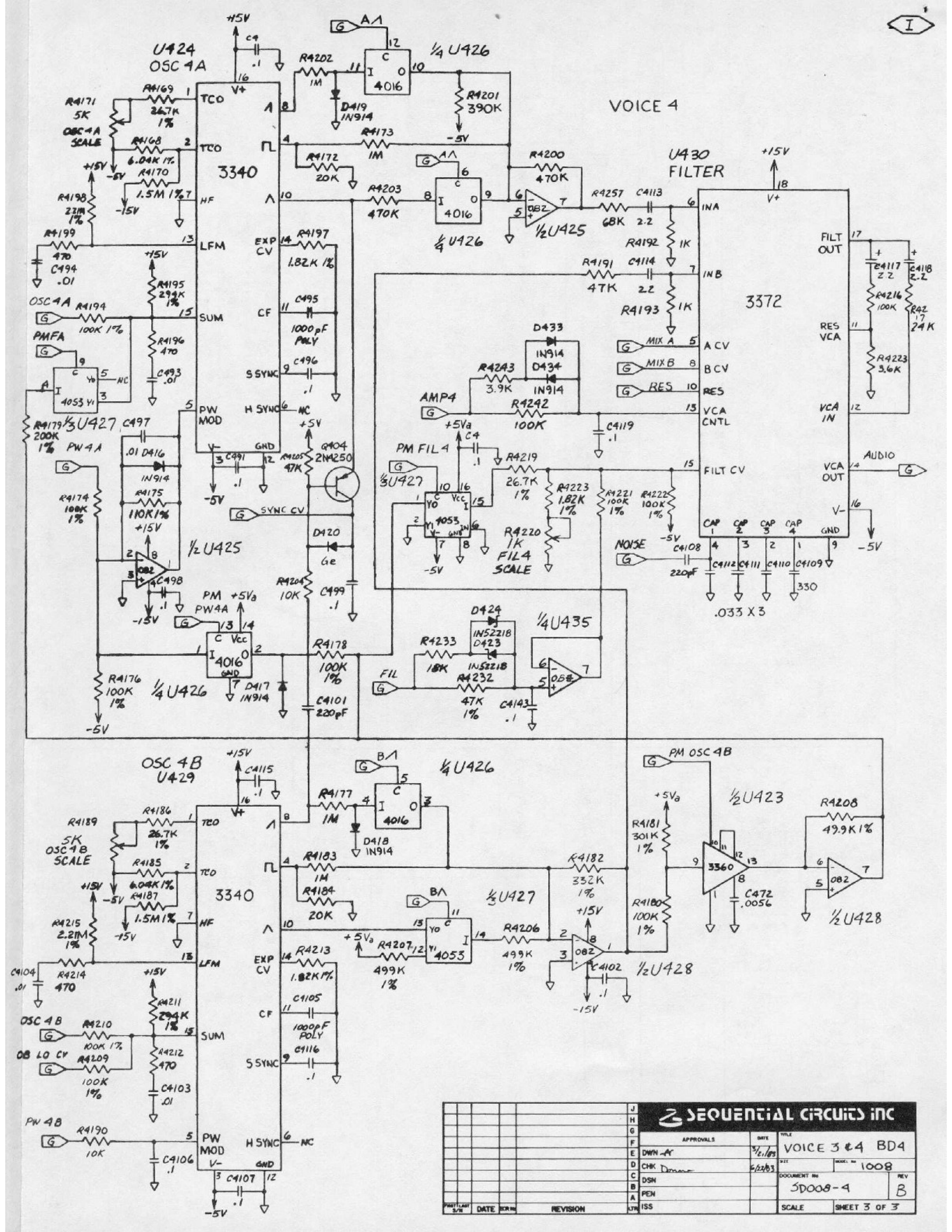

G
U446
DAC 71
CSB-I
U447
U448
U449
U450
U451
S/H DECODER
HC138
HC393
U452
TRANSLATOR
4504
U453
TRANSLATOR
U445
356
U436
U437
4051
TB402
TB404
R4255
332 1%
R4254
5.62K
1%
C4169
120 pF
R4236
10Ω
FIFO DATA
S/H A
S/H B
S/H C
S/H CLK
S/H CLR
SHIFT
U440
U441
U431
U432

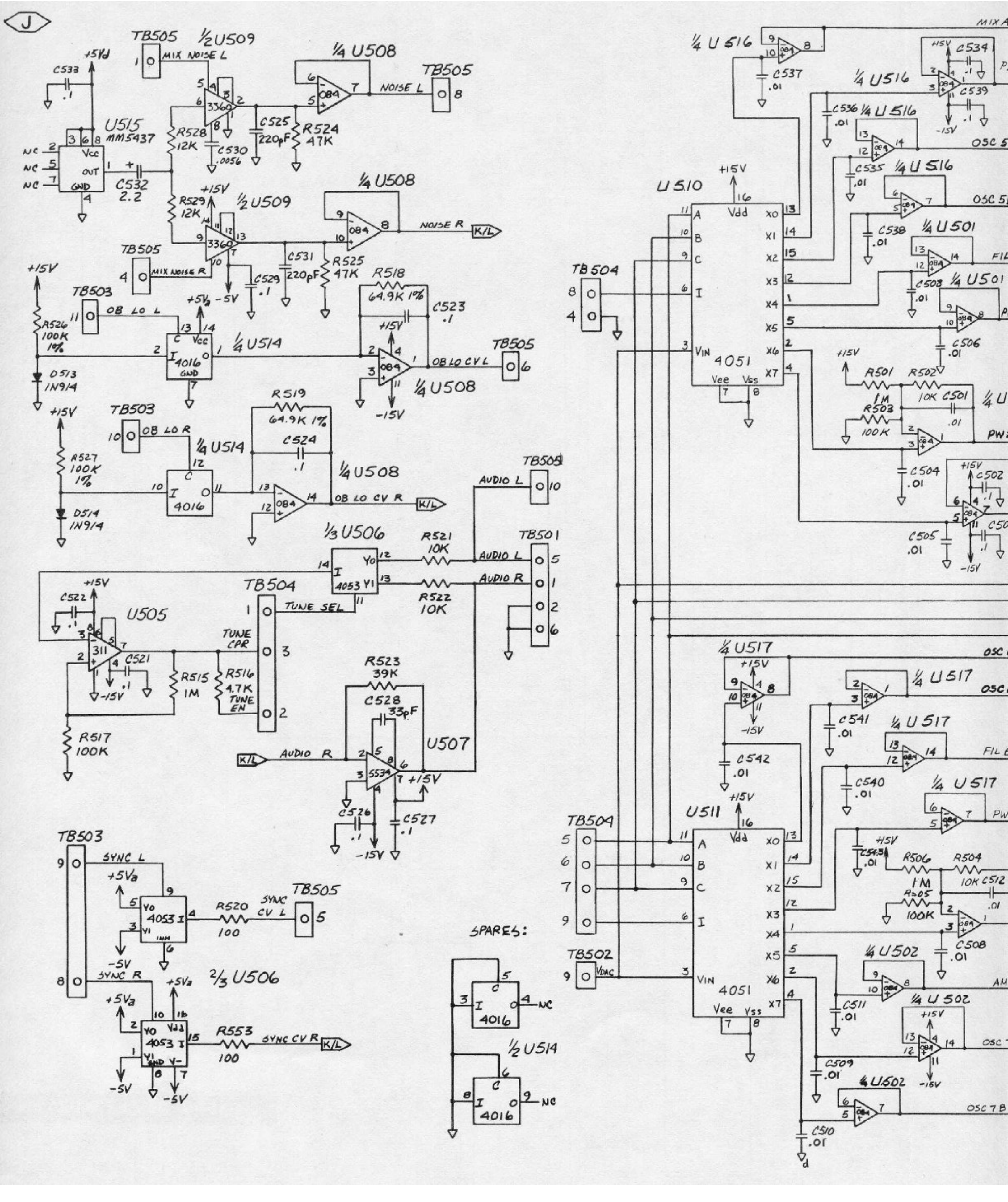

OSC1A
OSC1B
FIL1
PW1A
PW1B
AMP1
OSC2A
OSC 2B
FIL2
PW2A
PW2B
AMP2
OSC3A
OSC3B
FIL3
PW3A
ENZ
ENZ
VDAC
S/H A
S/H B
S/H C
EN3
U438
U439
4051
Vdd
Vss
Vee
VIN
PW3B
AMP3
OSC 4A
OSC 4B
FILT4
PW4A
PW4B
AMP4
RES L
MIX NOISE L
MIX BL
MIX AL
PM OSC BL
RES R
MIX NOISE R
MIX BR
U444
78L05
TB401
TB402
TB403
TB404
TB405
P401
PM PW A L
A∧L
B∧L
A∧L
B∧L
PM FIL L
PM FA L
TUNE SEL
TUNE EN
TUNE CPR
GND D
NC
PM PW A R
A∧R
B∧R
A∧R
B∧R
PM FIL R
PM FA R
SYNC R
SYNC L
B LO R
B LO L
SYNC CVL
OB LO CVL
NOISE L
AUDIO L
U454
5534
AUDIO L
R4247 39K
C4145
C4146 33pF
C4147
LAST USED: C4183 R257 D436
SEQUENTIAL CIRCUITS INC
VOICE BD 4
1008
SD008-1
B
SCALE
SHEET 3 OF 3
6/6/83
ADDED DESIGNATORS
REVISION
DO NOT SCALE DRAWING

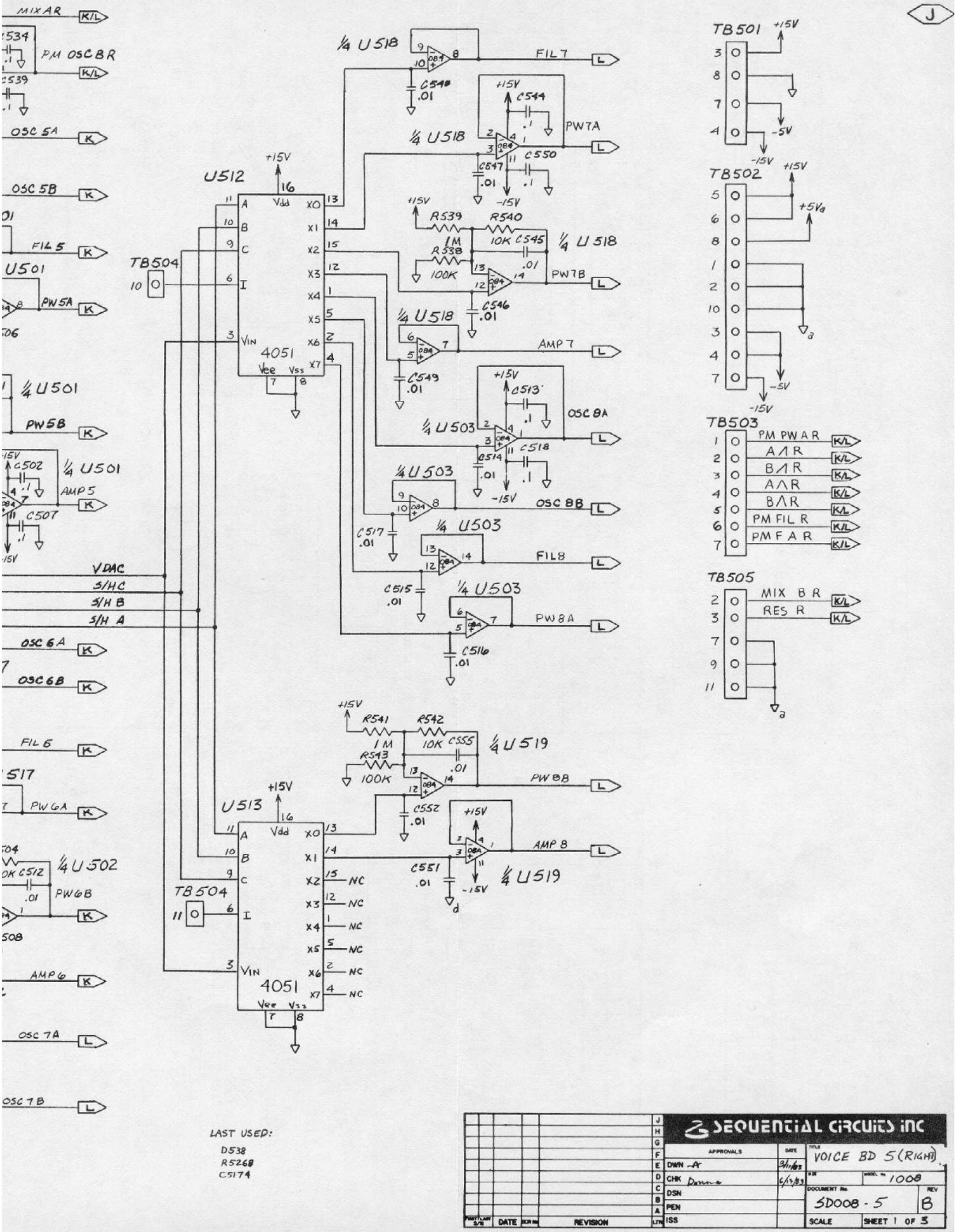

H
VOICE 1
U401
OSC 1 A
3340
U407
FILTER
3372
OSC 1 B
U406
3340
OSC 1 A SCALE
OSC 1 B SCALE
PW 1 A
PW 1 B
PM FIL 1
AMP 1
FIL 1
SYNC CV
NOISE
AUDIO 1
PM OSC 1B
PM +5Va
PW 1A
OB LO CV
+15V
-15V
+5V
+5Va
-5V
1/4 U403
1/2 U402
1/3 U404
1/4 U435
1/2 U408
1/2 U405
4016
4053
082
3360
.033 X 3

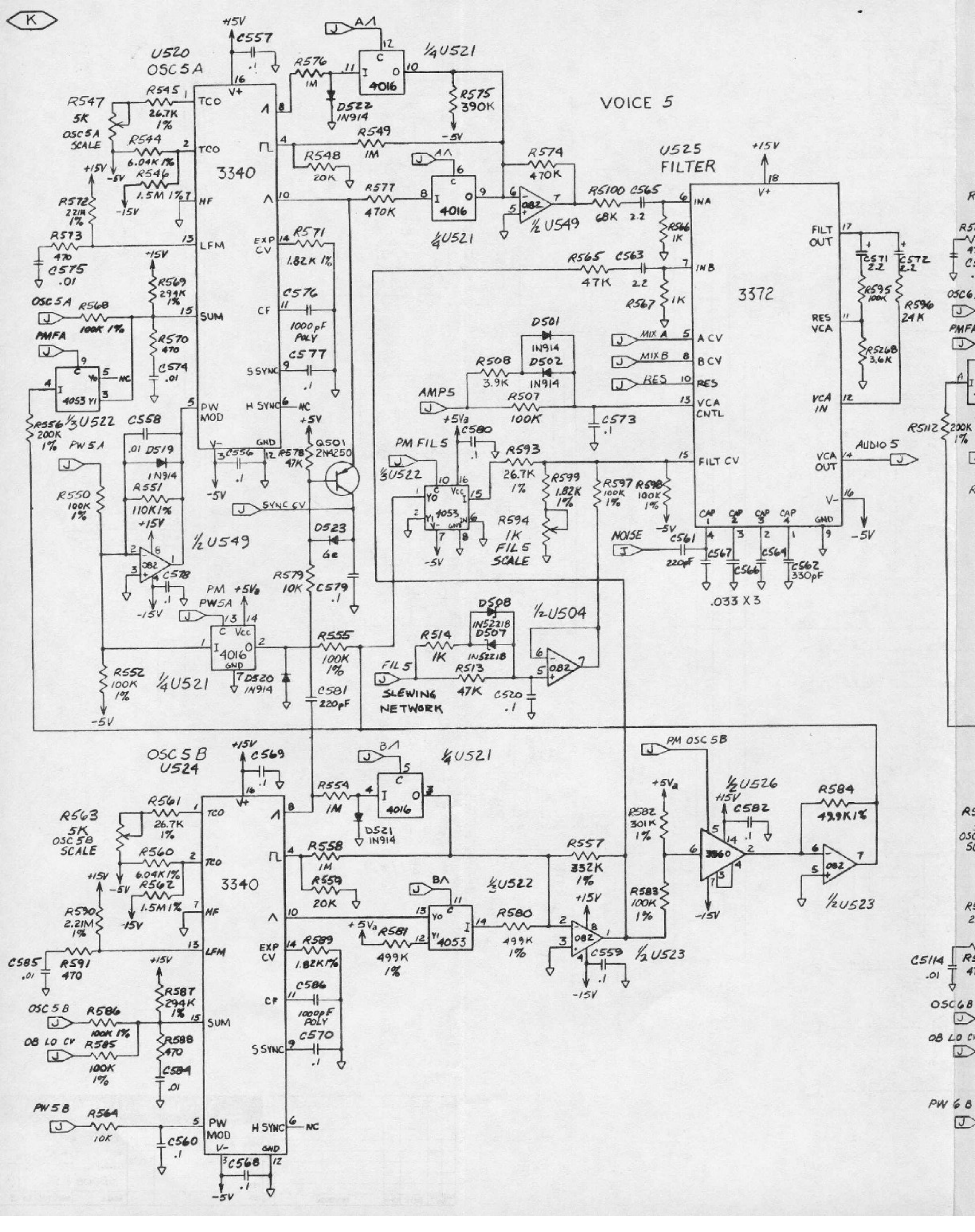

VOICE 2
U409
OSC 2A
3340
U415
FILTER
3372
OSC 2B
U414
3340
1/4 U411
1/2 U410
1/3 U412
1/2 U435
1/2 U408
1/2 U413
AUDIO 2
PM OSC 2B
PM FIL 2
AMP 2
NOISE
FIL 2
SYNC CV
PW 2A
PMFA
OSC 2A
OSC 2B
OB LO CV
PW 2B
.033 X 3
SEQUENTIAL CIRCUITS INC
VOICE 1 & 2
BD4
1008
SD008-4
REV B
SHEET 2 OF 3
DWN -PF 3/21/83
CHK 6/22/83
APPROVALS
REVISION
DATE

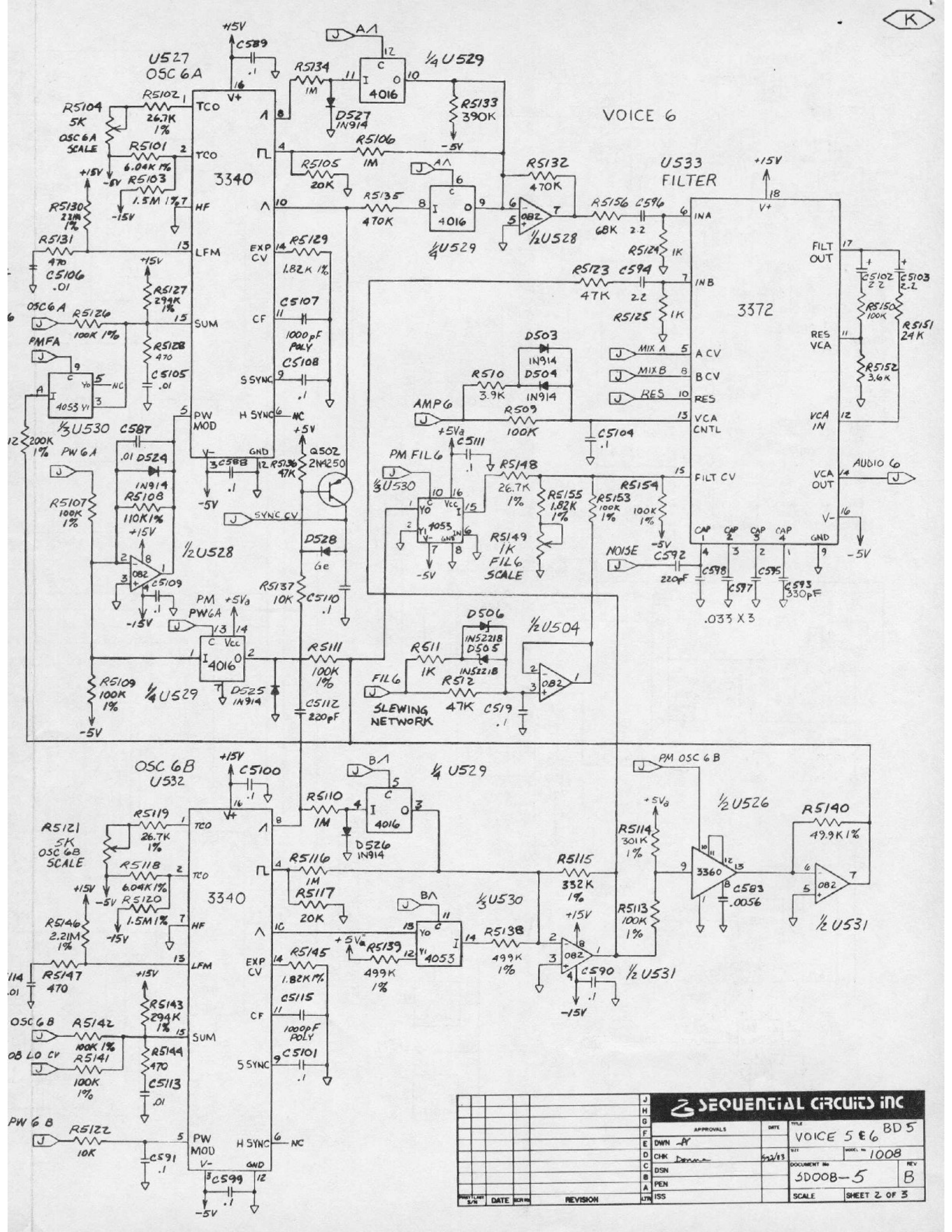

I
VOICE 3
U416
OSC 3A
3340
TCO
HF
LFM
SUM
PW MOD
V+
V-
GND
EXP CV
CF
S SYNC
H SYNC
NC
R4113 26.7K 1%
R4115 5K OSC 3A SCALE
R4112 6.04K 1%
R4114 1.5M 1%
R4140 2.21M 1%
R4141 470
C463 .01
R4137 294K 1%
OSC 3A
R4136 100K 1%
R4138 470
C462 .01
PMFA
4053
1/3 U419
R4123 200K 1%
PW 3A
C466 .01
D411 1N914
R4118 100K 1%
R4119 110K 1%
1/2 U417
082
C467 .1
C461 .1
R4144 1M
D414 1N914
1/4 U418
4016
R4143 390K
R4117 1M
R4116 20K
R4139 1.82K 1%
C464 1000pF POLY
C465 .1
C460 .1
R4145 470K
R4142 470K
R4147 47K
Q403 2N4250
SYNC CV
D415 Ge
C468 .1
R4146 10K
PM PW3A
+5Va
R4122 100K 1%
D412 1N914
R4120 100K 1%
C470 220pF
U422
FILTER
3372
INA
INB
A CV
B CV
RES
VCA CNTL
FILT CV
FILT OUT
RES VCA
VCA IN
VCA OUT
CAP 1
CAP 2
CAP 3
CAP 4
R4188 68K
C483 2.2
R4134 1K
R4133 47K
C482 2.2
R4135 1K
C488 2.2
C489 2.2
R4160 100K
R4161 24K
R4167 3.6K
MIX A
MIX B
D434 1N914
D433 1N914
R4243 3.9K
AMP 3
R4244 100K
C490 .1
AUDIO
PM FIL 3
C469 .1
R4163 26.7K 1%
R4167 1.82K 1%
R4164 1K FIL 3 SCALE
R4165 100K 1%
R4166 100K 1%
NOISE
C479 220pF
C487
C486
C485
C484 330
.033 X 3
D421 1N5221B
D422 1N5221B
R4230 18K
1/4 U435
FIL
R4231 47K 1%
C4141 .1
OSC 3B
U421
C480 .1
R4128 26.7K 1%
R4130 5K OSC 3B SCALE
R4127 6.04K 1%
R4129 1.5M 1%
R4159 2.21M 1%
R4158 470
C475 .01
R4155 294K 1%
R4154 100K 1%
OB LO CV
R4153 100K 1%
R4156 470
C474 .01
PW 3B
R4132 10K
C477 .1
C478 .1
R4121 1M
D413 1N914
R4125 1M
R4126 20K
R4157 1.82K 1%
C476 1000pF POLY
C481 .1
R4149 499K 1%
R4148 499K 1%
PM OSC 3B
R4150 301K 1%
R4151 100K 1%
R4124 332K 1%
1/2 U423
3360
C471 .1
R4152 49.9K 1%
1/2 U420
C473 .1
+15V
-15V
+5V
-5V

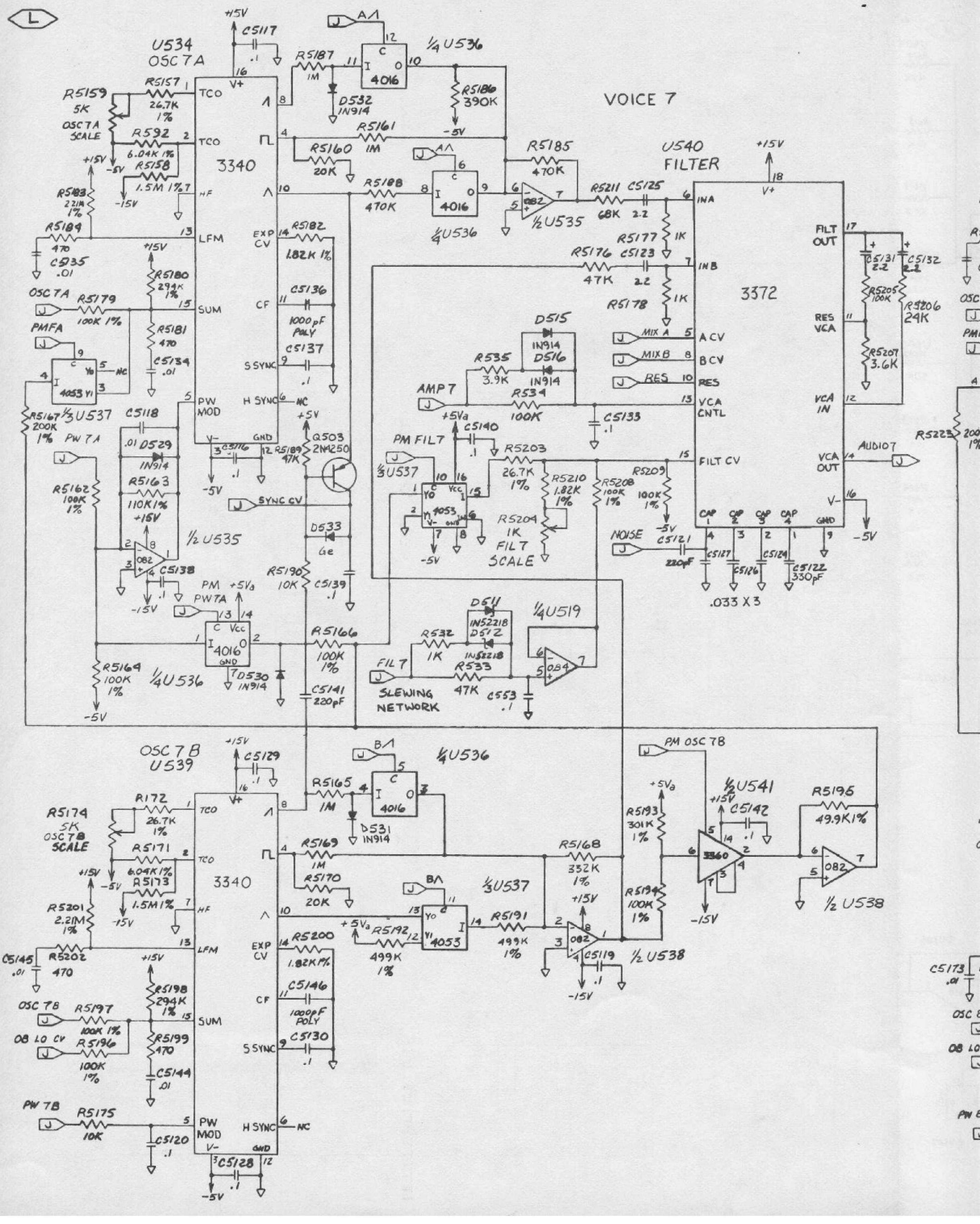

VOICE 4
U424
OSC 4A
3340
U430
FILTER
3372
OSC 4B
U429
3340
PM OSC 4B
AMP4
PM FIL4
PW4A
PW 4B
SYNC CV
NOISE
.033 X 3
SEQUENTIAL CIRCUITS INC
VOICE 3 & 4 BD4
1008
5D008-4
B
SCALE
SHEET 3 OF 3
DSN
PEN
ISS
DWN AY
CHK Dave
5/21/83
6/22/83


J
TB505
1/2 U509
MIX NOISE L
1/4 U508
NOISE L
U515
MM5437
C532
2.2
R528
12K
R529
12K
C530
.0056
C525
220pF
R524
47K
NOISE R
K/L
C531
220pF
R525
47K
MIX NOISE R
C529
.1
R518
64.9K 1%
C523
.1
TB503
OB LO L
R526
100K
1%
D513
1N914
1/4 U514
4016
OB LO CV L
R519
64.9K 1%
C524
OB LO R
R527
100K
1%
D514
1N914
OB LO CV R
1/3 U506
4053
R521
10K
AUDIO L
R522
10K
AUDIO R
TB501
TB504
TUNE SEL
TUNE CPR
TUNE EN
U505
311
C522
C521
R515
1M
R516
4.7K
R517
100K
R523
39K
C528
33pF
U507
5534
C526
C527
SYNC L
R520
100
SYNC CV L
SYNC R
2/3 U506
R553
100
SYNC CV R
SPARES:
1/2 U514
U510
4051
U511
TB502
VDAC
1/4 U516
C537
C534
C539
C536
C535
OSC 5
1/4 U501
C538
FIL
C508
R501
R502
10K
C501
1M
R503
100K
PW
C504
C502
C505
1/4 U517
C541
C542
C540
R506
R504
C512
R505
C543
1/4 U502
C511
AM
C509
C510
OSC 7B
MIX A

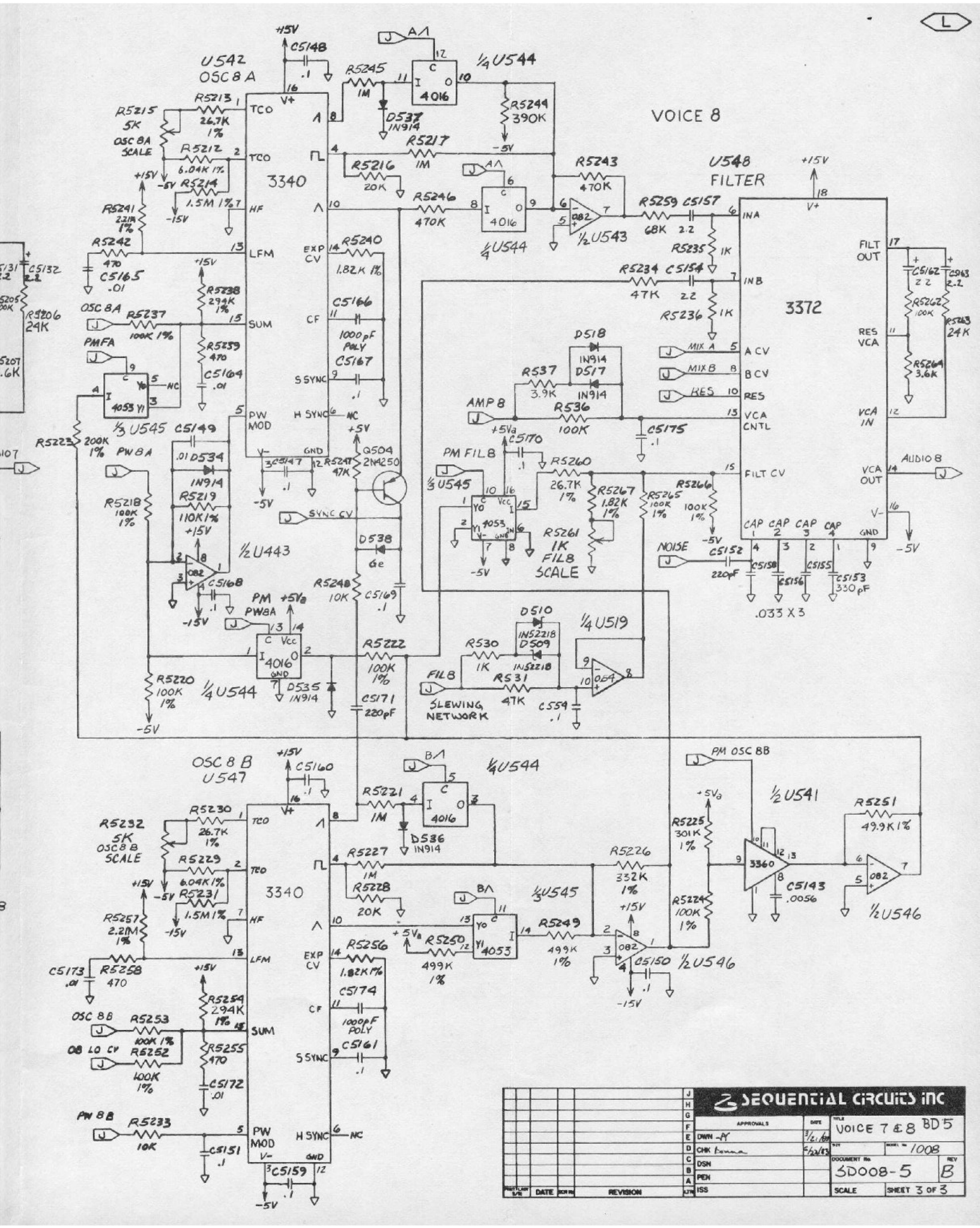

MIX AR
PM OSC BR
OSC 5A
OSC 5B
FIL 5
PW 5A
¼ U501
PW 5B
AMP 5
VDAC
S/H C
S/H B
S/H A
OSC 6A
OSC 6B
FIL 6
PW 6A
¼ U502
PW 6B
AMP 6
OSC 7A
OSC 7B
¼ U518
FIL 7
PW 7A
PW 7B
AMP 7
¼ U503
OSC 8A
OSC 8B
FIL 8
PW 8A
¼ U519
PW 8B
AMP 8
U512
U513
4051
TB504
TB501
TB502
TB503
TB505
PM PW A R
A Λ R
B Λ R
A V R
B V R
PM FIL R
PM F A R
MIX B R
RES R
+15V
-15V
+5V
-5V
LAST USED:
D538
R526B
C5174
SEQUENTIAL CIRCUITS INC
VOICE BD 5 (RIGHT)
1008
5D008 - 5
B
SCALE
SHEET 1 OF 3

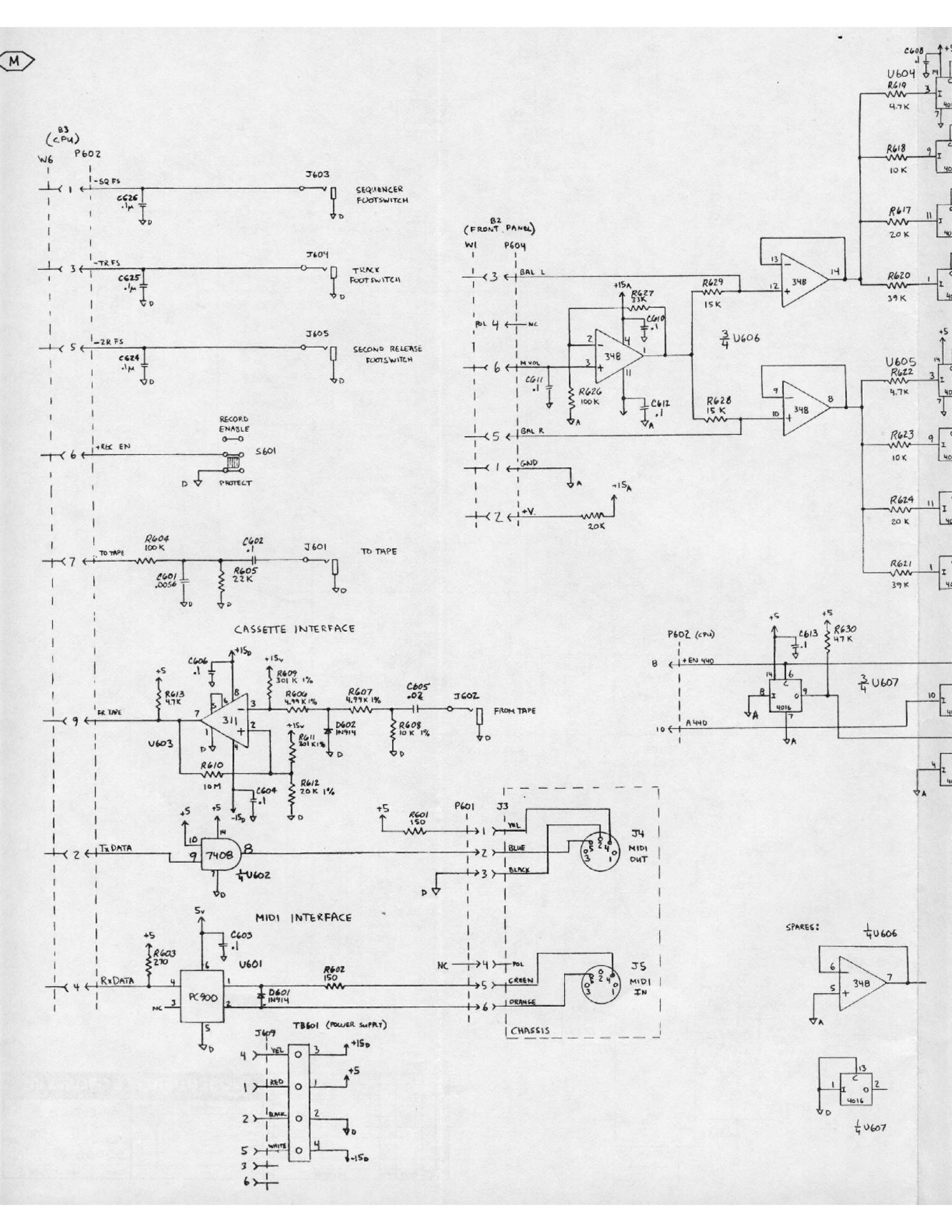

K
VOICE 5
U520
OSC 5A
3340
U524
OSC 5B
U525
FILTER
3372
AUDIO 5
NOISE
SLEWING
NETWORK
.033 X 3
PM OSC 5B
PW 5A
PW 5B
OSC 5A
OSC 5B
PMFA
AMP5
MIX A
MIX B
RES
SYNC CV
PM FIL 5
FIL 5
OB LO CV
1/4 U521
1/2 U549
1/3 U522
1/2 U504
1/2 U526
1/2 U523
R547
5K
OSC 5A SCALE
R563
5K
OSC 5B SCALE
R594
1K
FIL 5 SCALE

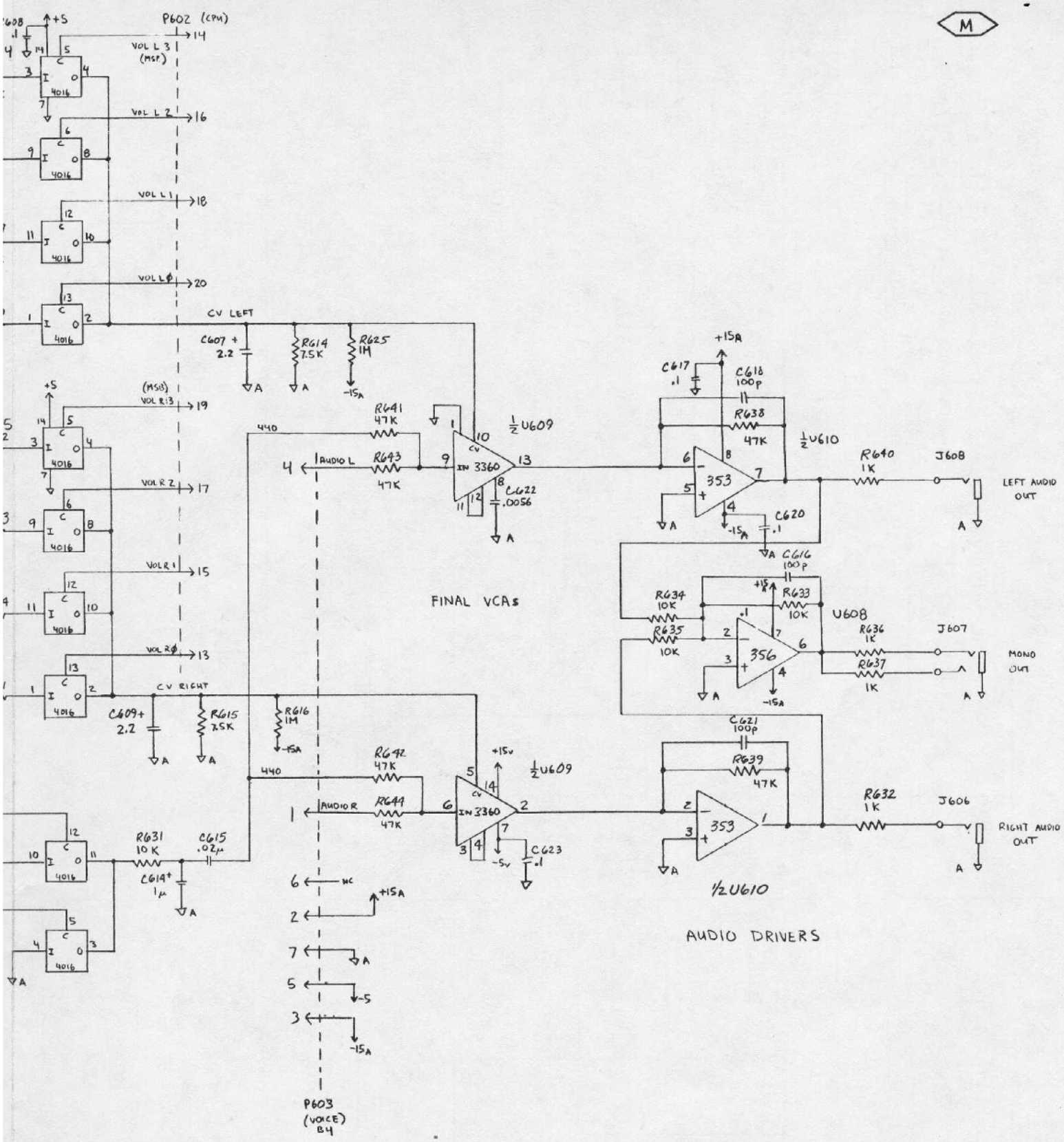

K
VOICE 6
U527
OSC 6A
3340
U533
FILTER
3372
OSC 6B
U532
SEQUENTIAL CIRCUITS INC
VOICE 5 & 6 BD 5
1008
5D008-5
B
SHEET 2 OF 3



VOICE 7
U534
OSC 7A
3340
U540
FILTER
3372
OSC 7B
U539
3340
SLEWING NETWORK
AMP 7
PM FIL7
FIL 7
NOISE
AUDIO7
MIX A
MIX B
RES
SYNC CV
PMFA
PW 7A
PM PWTA
OSC 7A
OSC 7B
OB LO CV
PW 7B
PM OSC 7B
R5159 5K OSC 7A SCALE
R5174 5K OSC 7B SCALE
R5204 1K FIL 7 SCALE
Q503 2N4250
.033 X 3
1/2 U535
1/4 U536
1/3 U537
1/4 U519
1/2 U541
1/2 U538


VOICE 8
U542
OSC 8 A
3340
U548
FILTER
3372
OSC 8 B
U547
OSC 8A SCALE
OSC 8B SCALE
PM FILB
AMP 8
FILB SLEWING NETWORK
PW8A
PW 8B
OSC 8B
OB LO CV
PM OSC 8B
PM +5Va
NOISE
AUDIO 8
.033 X 3
1/4 U544
1/2 U543
1/3 U545
1/2 U443
1/4 U519
1/2 U541
1/2 U546
1/3 U545
SEQUENTIAL CIRCUITS INC
VOICE 7 & 8 BD5
3D008-5
REV B
SHEET 3 OF 3

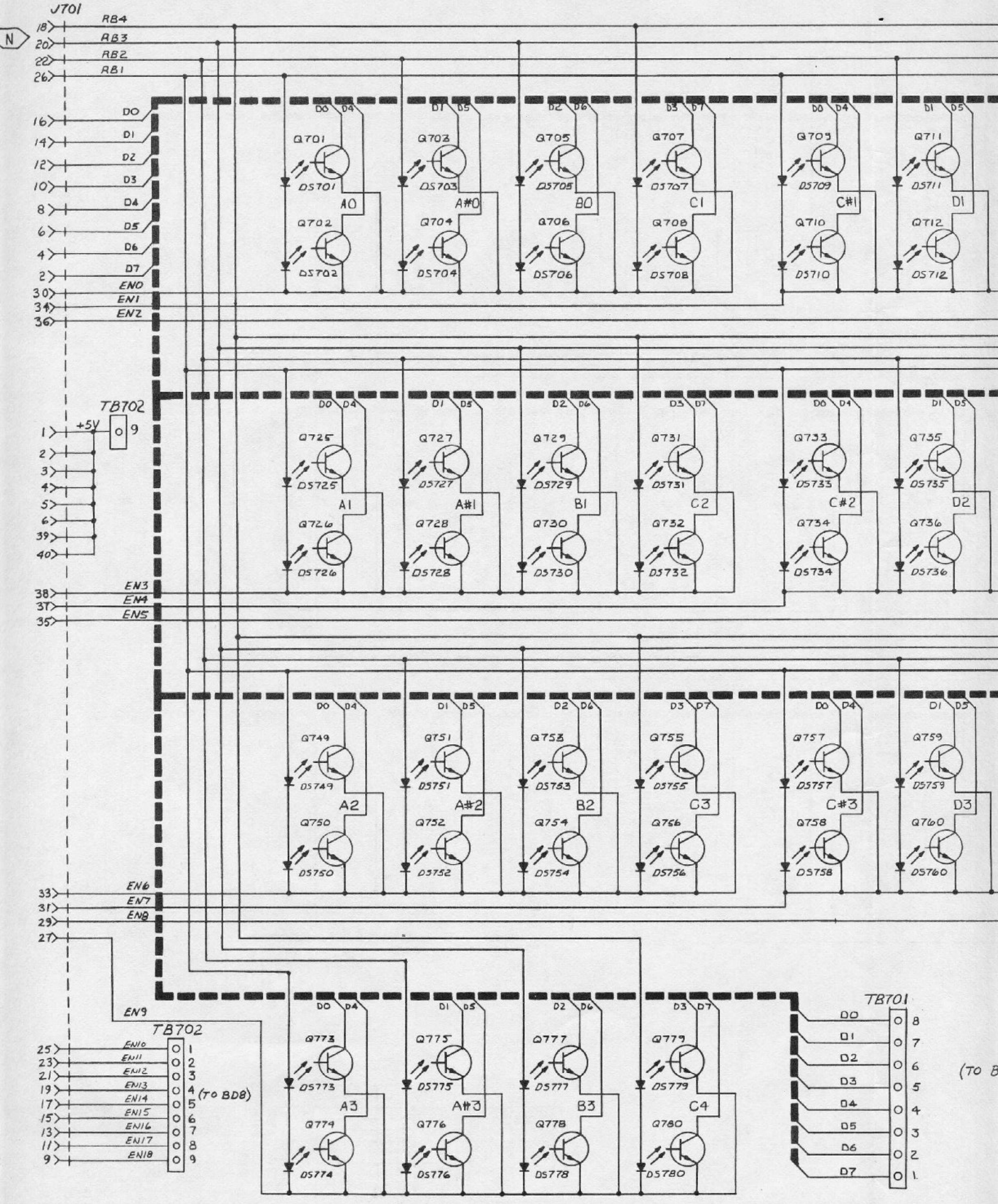

M
B3 (CPU)
W6
P602
-SQ FS
J603
SEQUENCER FOOTSWITCH
C626 .1μ
-TR FS
J604
TRACK FOOTSWITCH
C625 .1μ
-2R FS
J605
SECOND RELEASE FOOTSWITCH
C624 .1μ
RECORD ENABLE
+REC EN
S601
PROTECT
TO TAPE
R604 100K
C602 .1
J601
TO TAPE
C601 .0056
R605 22K
CASSETTE INTERFACE
FR TAPE
U603
311
C606 .1
+15D
+15V
R609 301K 1%
R606 4.99K 1%
R607 4.99K 1%
C605 .02
J602
FROM TAPE
R613 4.7K
R611 301K 1%
D602 IN914
R608 10K 1%
R610 10M
C604 .1
R612 20K 1%
-15D
Tx DATA
7408
+U602
P601
J3
R601 150
YEL
BLUE
BLACK
J4 MIDI OUT
MIDI INTERFACE
5V
C603 .1
R603 270
U601
Rx DATA
PC900
R602 150
D601 IN914
NC
POL
GREEN
ORANGE
J5 MIDI IN
CHASSIS
TB601 (POWER SUPPLY)
J609
YEL
RED
BLACK
WHITE
B2 (FRONT PANEL)
W1
P604
BAL L
POL
NC
M VOL
BAL R
GND
+V.
+15A
R627 33K
C610 .1
R626 100K
C611 .1
C612 .1
R629 15K
R628 15K
20K
348
¾ U606
U605
R622 4.7K
R623 10K
R624 20K
R621 39K
U604
R619 4.7K
R618 10K
R617 20K
R620 39K
C608 .1
P602 (CPU)
+EN 440
A 440
C613 .1
R630 47K
¾ U607
SPARES:
¼ U606
¼ U607
4016

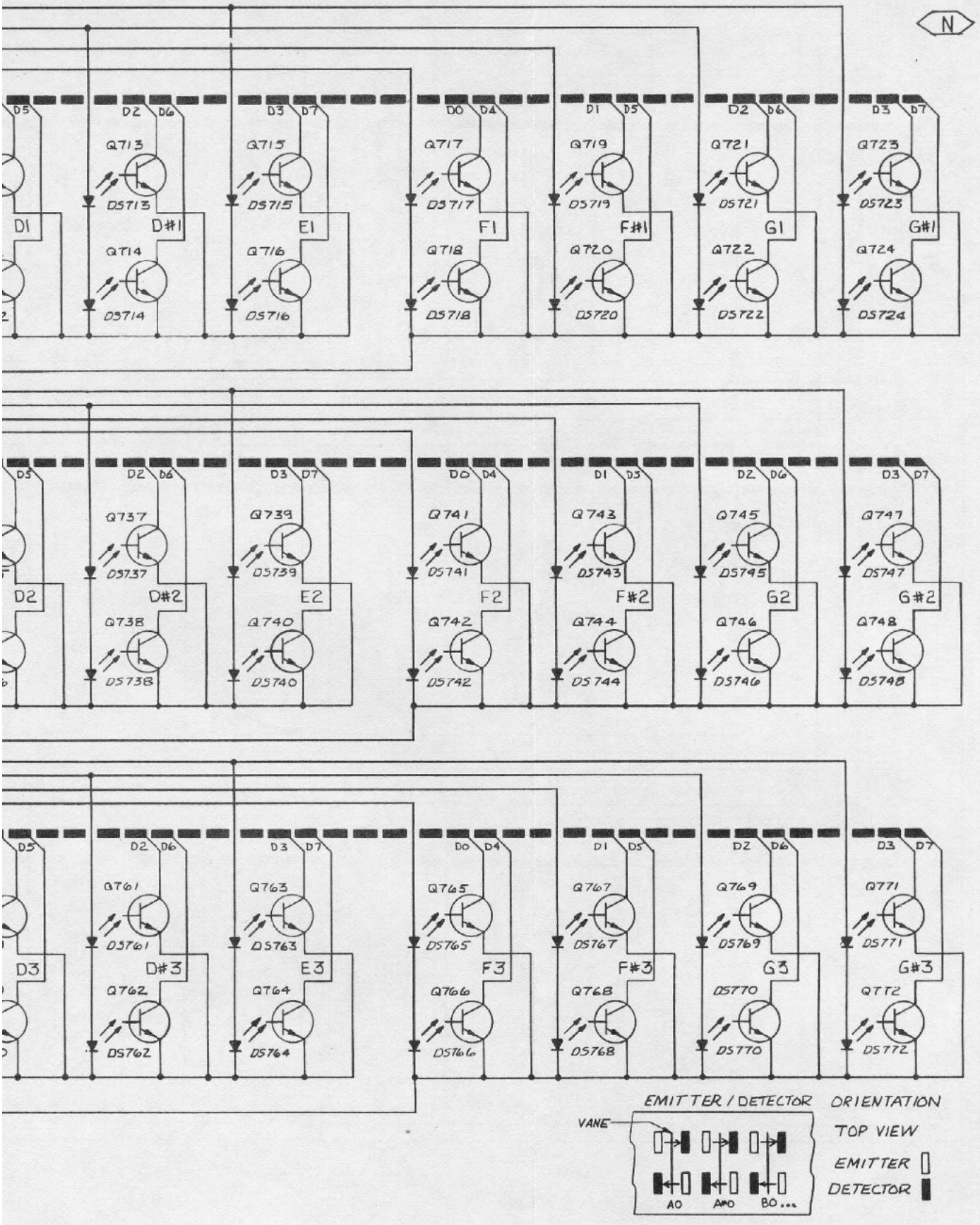


					J	SEQUENTIAL CIRCUITS INC
					H	
					G	
					F	APPROVALS / DATE
					E	DWN DAVE 1/6/82
					D	CHK Donna 6/3/83
					C	DSN
			5-12-83	DELETE PULLUPS; 356 AS 5532	B	PEN
					A	ISS
			DATE	REVISION	LTR	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES MATERIAL FINISH DO NOT SCALE DRAWING

TITLE: BOARD 6 SCHEMATIC
SIZE: — MODEL No: 1008
DOCUMENT No: SD008-6 REV: B
SCALE: — SHEET 1 OF 1


J701
RB4
RB3
RB2
RB1
D0
D1
D2
D3
D4
D5
D6
D7
EN0
EN1
EN2
EN3
EN4
EN5
EN6
EN7
EN8
EN9
TB702
+5V
TB701
(TO BD8)
(TO B
A0
A#0
B0
C1
C#1
D1
A1
A#1
B1
C2
C#2
D2
A2
A#2
B2
C3
C#3
D3
A3
A#3
B3
C4



(TO BD 8)

						J
						H
						G
						F
						E
						D
						C
		5-4-85		40-PIN CONNECTOR PIN #'S		B
DO NOT SCALE DRAWING		DATE		REVISION		A

SEQUENTIAL CIRCUITS INC

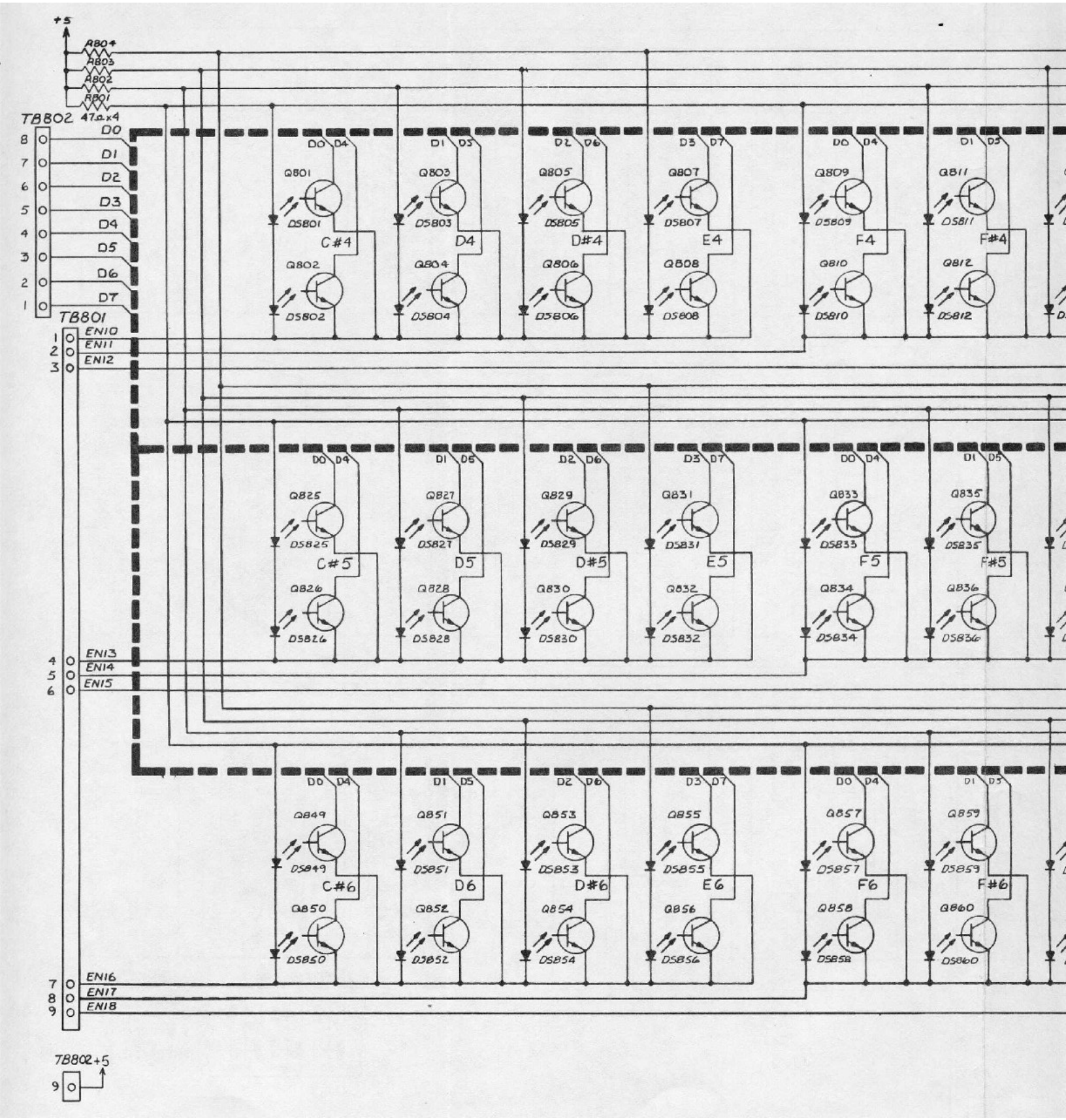
APPROVALS	DATE
DWN AY	7-2-85
CHK Dennis	8/13/85
DSN	
PEN	
ISS	

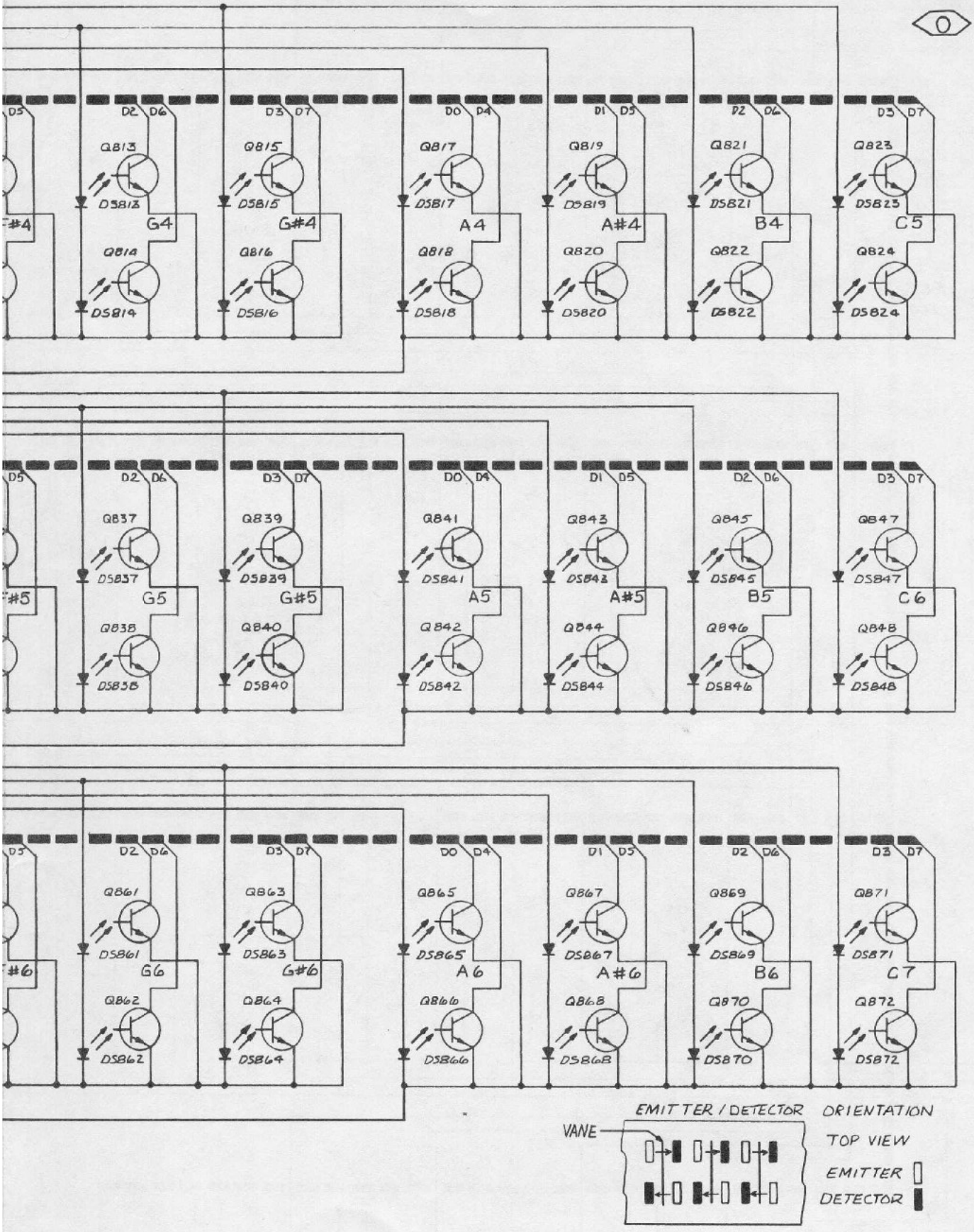
TITLE: OPTICAL BD 7

SIZE: | MODEL No. 1008

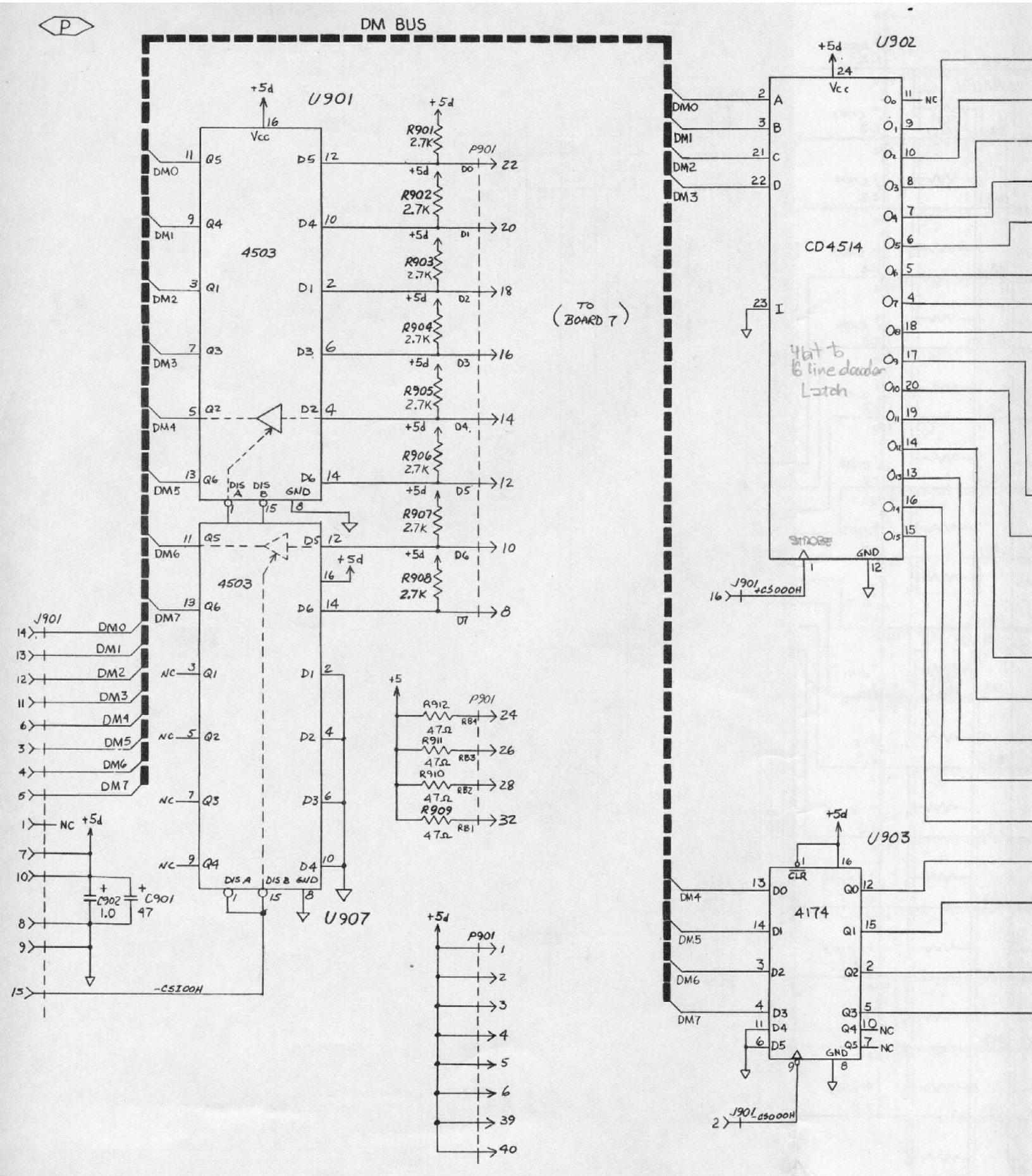
DOCUMENT No. 8D008-7 | REV. B

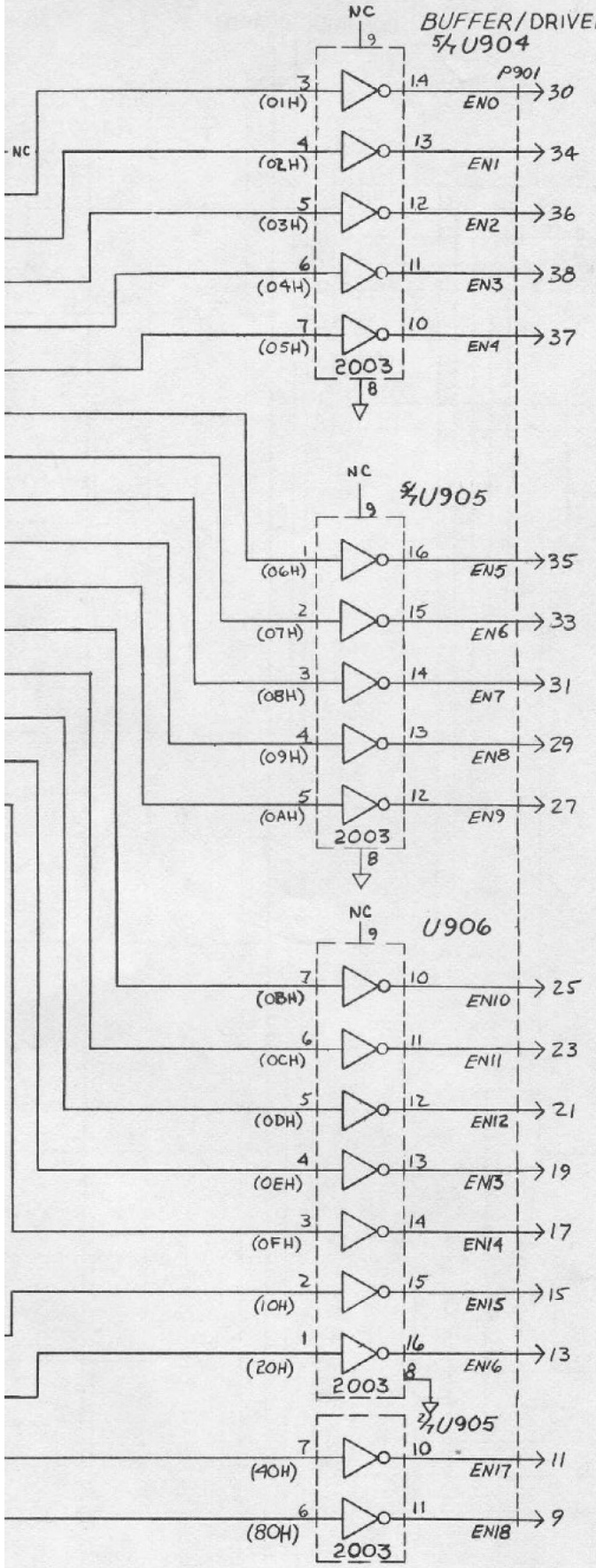
SCALE | SHEET 1 OF 1


+5
RB04
RB03
RB02
RB01
TB802 47Ω×4
TB801
D0
D1
D2
D3
D4
D5
D6
D7
EN10
EN11
EN12
EN13
EN14
EN15
EN16
EN17
EN18
Q801
Q802
DS801
DS802
C#4
Q803
Q804
DS803
DS804
D4
Q805
Q806
DS805
DS806
D#4
Q807
Q808
DS807
DS808
E4
Q809
Q810
DS809
DS810
F4
Q811
Q812
DS811
DS812
F#4
Q825
Q826
DS825
DS826
C#5
Q827
Q828
DS827
DS828
D5
Q829
Q830
DS829
DS830
D#5
Q831
Q832
DS831
DS832
E5
Q833
Q834
DS833
DS834
F5
Q835
Q836
DS835
DS836
F#5
Q849
Q850
DS849
DS850
C#6
Q851
Q852
DS851
DS852
D6
Q853
Q854
DS853
DS854
D#6
Q855
Q856
DS855
DS856
E6
Q857
Q858
DS857
DS858
F6
Q859
Q860
DS859
DS860
F#6
TB802+5



							J	SEQUENTIAL CIRCUITS INC
							H	
							G	
							F	APPROVALS / DATE
							E	DWN AY 2-3-83
							D	CHK Donna 2/3/83
							C	DSN
							B	PEN
							A	ISS
								TITLE: OPTICAL BD8
								SIZE: — MODEL No. 1008
								DOCUMENT No. SD008-8 REV A
								SCALE SHEET 1 OF 1
DO NOT SCALE DRAWING				DATE		REVISION		

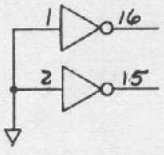

P
DM BUS
U901
4503
U902
CD4514
4bit to 16 line decoder Latch
U903
4174
U907
4503
Vcc
GND
DIS A
DIS B
+5d
R901 2.7K
R902 2.7K
R903 2.7K
R904 2.7K
R905 2.7K
R906 2.7K
R907 2.7K
R908 2.7K
P901
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
J901
-CS1OOH
-CS000H
C902 1.0
C901 47
R912 47Ω
R911 47Ω
R910 47Ω
R909 47Ω
RB4
RB3
RB2
RB1
(TO BOARD 7)
NC



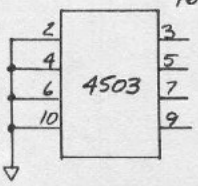
(TO BOARD T)

SPARES:

2/7 U904



4/6 U907



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .X							
MATERIAL							
FINISH							
DO NOT SCALE DRAWING	SHEET LAST S/N	DATE	ECR No	REVISION			

SEQUENTIAL CIRCUITS INC

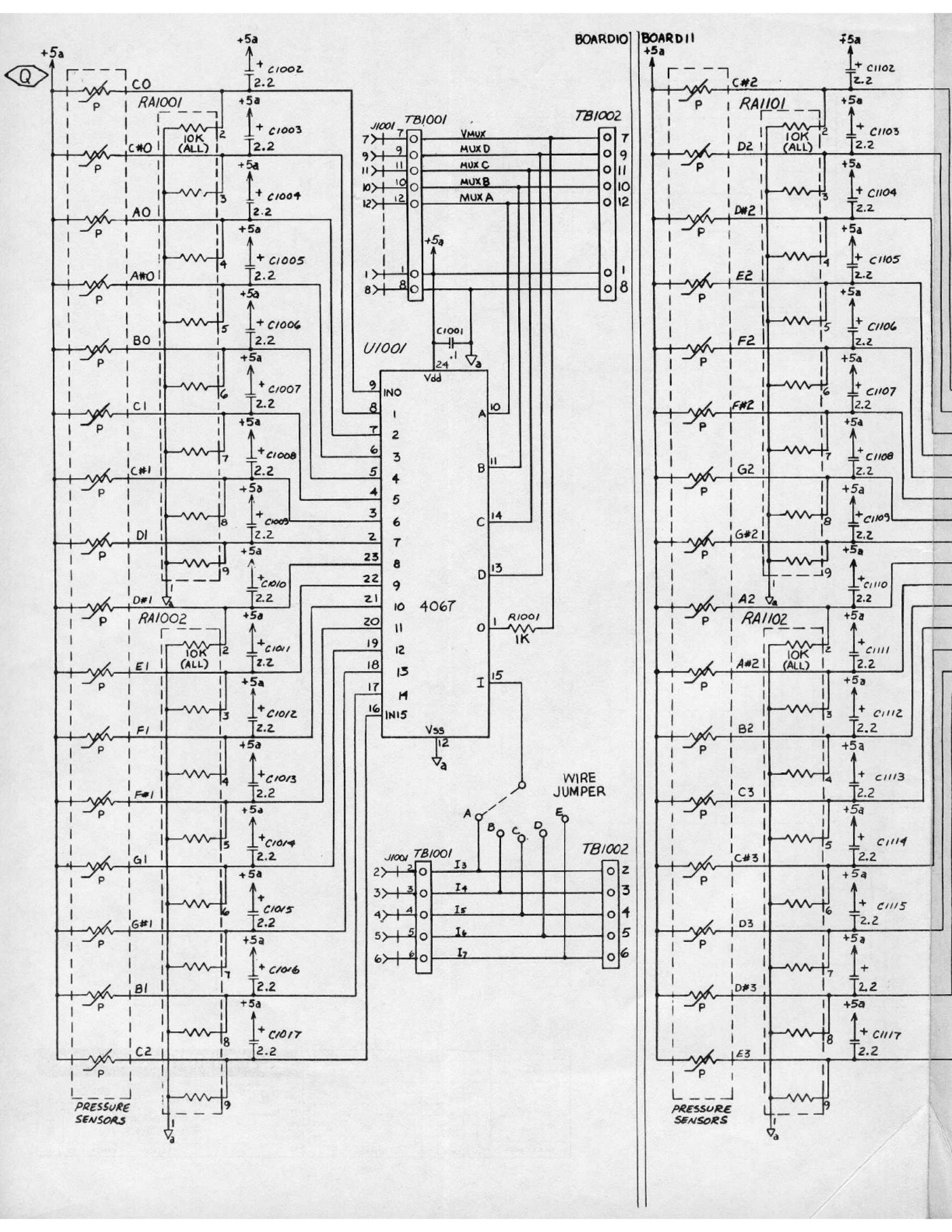
APPROVALS	DATE
DWN AY	2/6/85
CHK D	5/13/85
DSN	
PEN	
ISS	

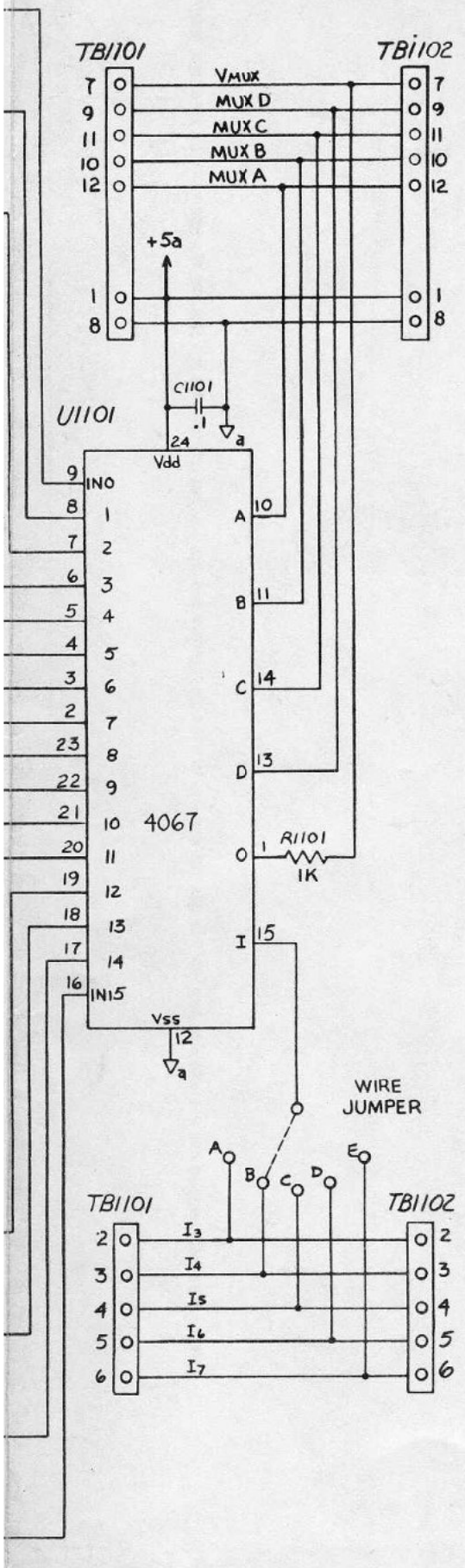
TITLE: OPTICAL BD 9

SIZE | MODEL No. 1008

DOCUMENT No. SD008-9 | REV. B

SCALE | SHEET 1 OF 1


BOARD I0
BOARD I1
+5a
Q
C0
C#0
A0
A#0
B0
C1
C#1
D1
D#1
E1
F1
F#1
G1
G#1
B1
C2
RA1001
RA1002
10K (ALL)
C1002
C1003
C1004
C1005
C1006
C1007
C1008
C1009
C1010
C1011
C1012
C1013
C1014
C1015
C1016
C1017
2.2
PRESSURE SENSORS
J1001
TB1001
TB1002
VMUX
MUX D
MUX C
MUX B
MUX A
C1001
.1
U1001
Vdd
Vss
IN0
IN15
4067
A
B
C
D
I
R1001
1K
WIRE JUMPER
I3
I4
I5
I6
I7
C#2
D2
D#2
E2
F2
F#2
G2
G#2
A2
A#2
B2
C3
C#3
D3
D#3
E3
RA1101
RA1102
C1102
C1103
C1104
C1105
C1106
C1107
C1108
C1109
C1110
C1111
C1112
C1113
C1114
C1115
C1117



							J
							H
							G
							F
							E
							D
							C
							B
							A
			5983		CHANGED JMPR DESIGNATOR		
			DATE		REVISION		

SEQUENTIAL CIRCUITS INC

APPROVALS	DATE
DSN AT	2/7/83
CHK Dmore	4/13/83
DEN	
PRN	
MFG	

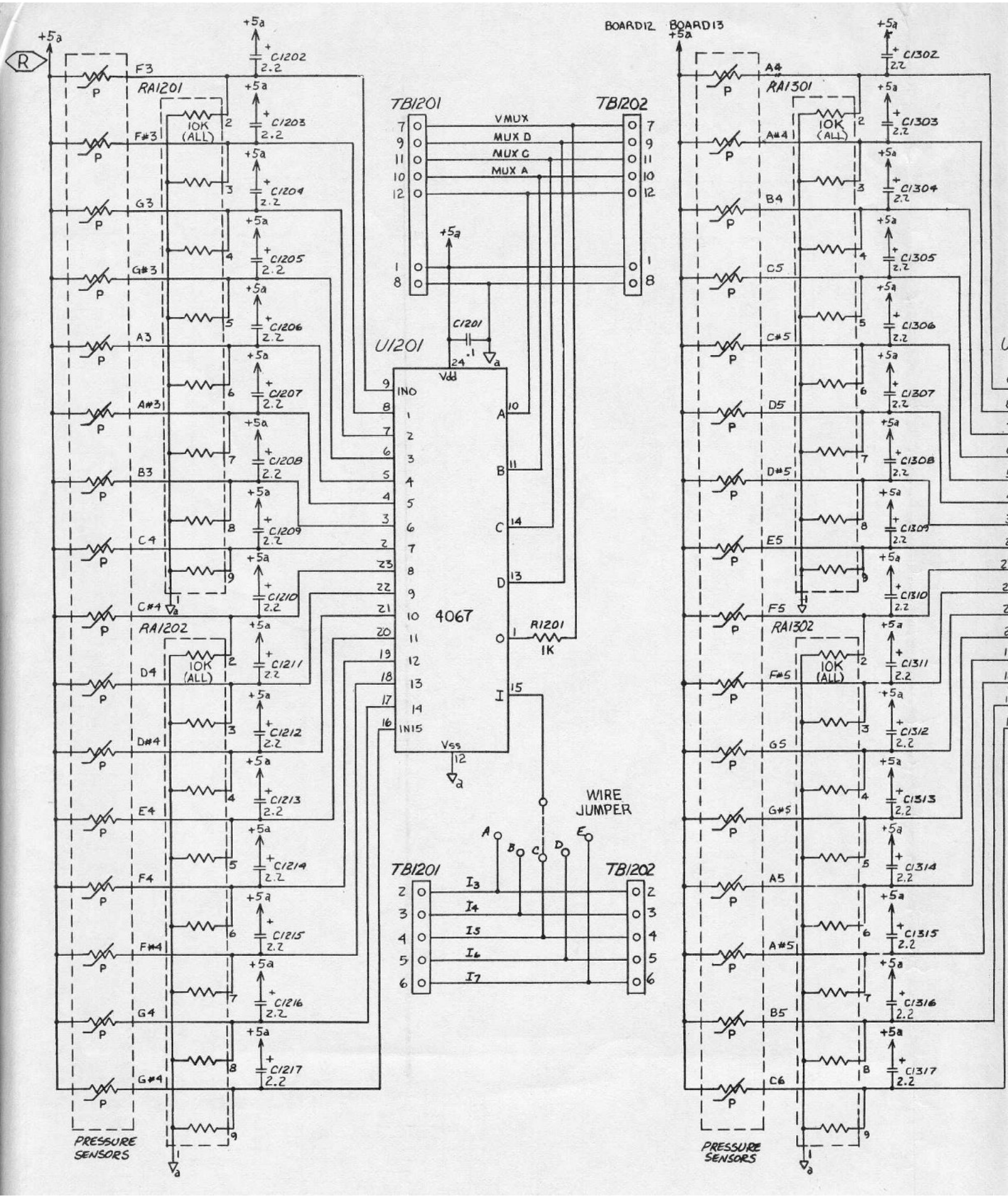
TITLE: PRESSURE BOARDS

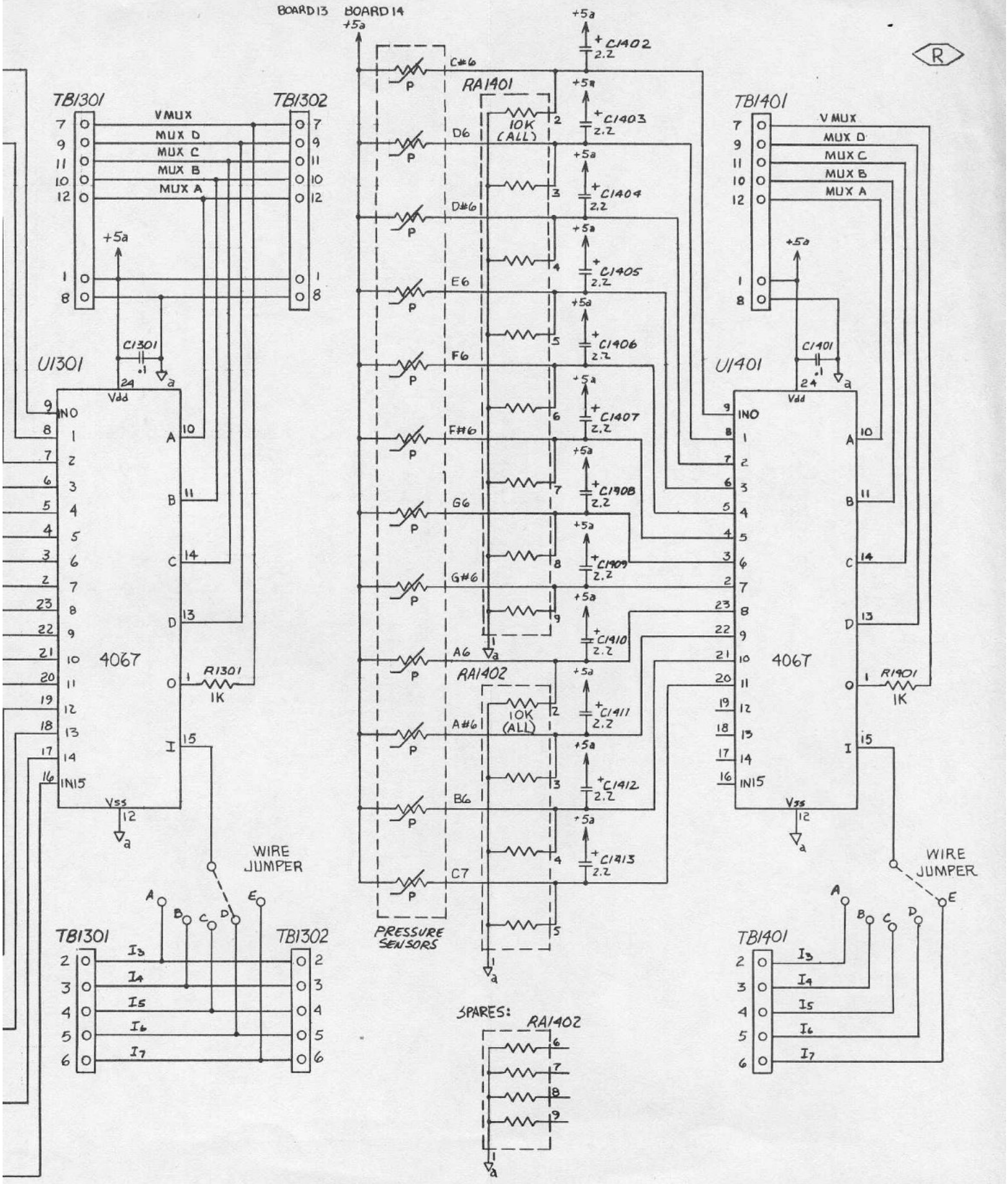
SIZE: B | DWG. NO. 1008

DOCUMENT NO. SD008-10/11 | REV B

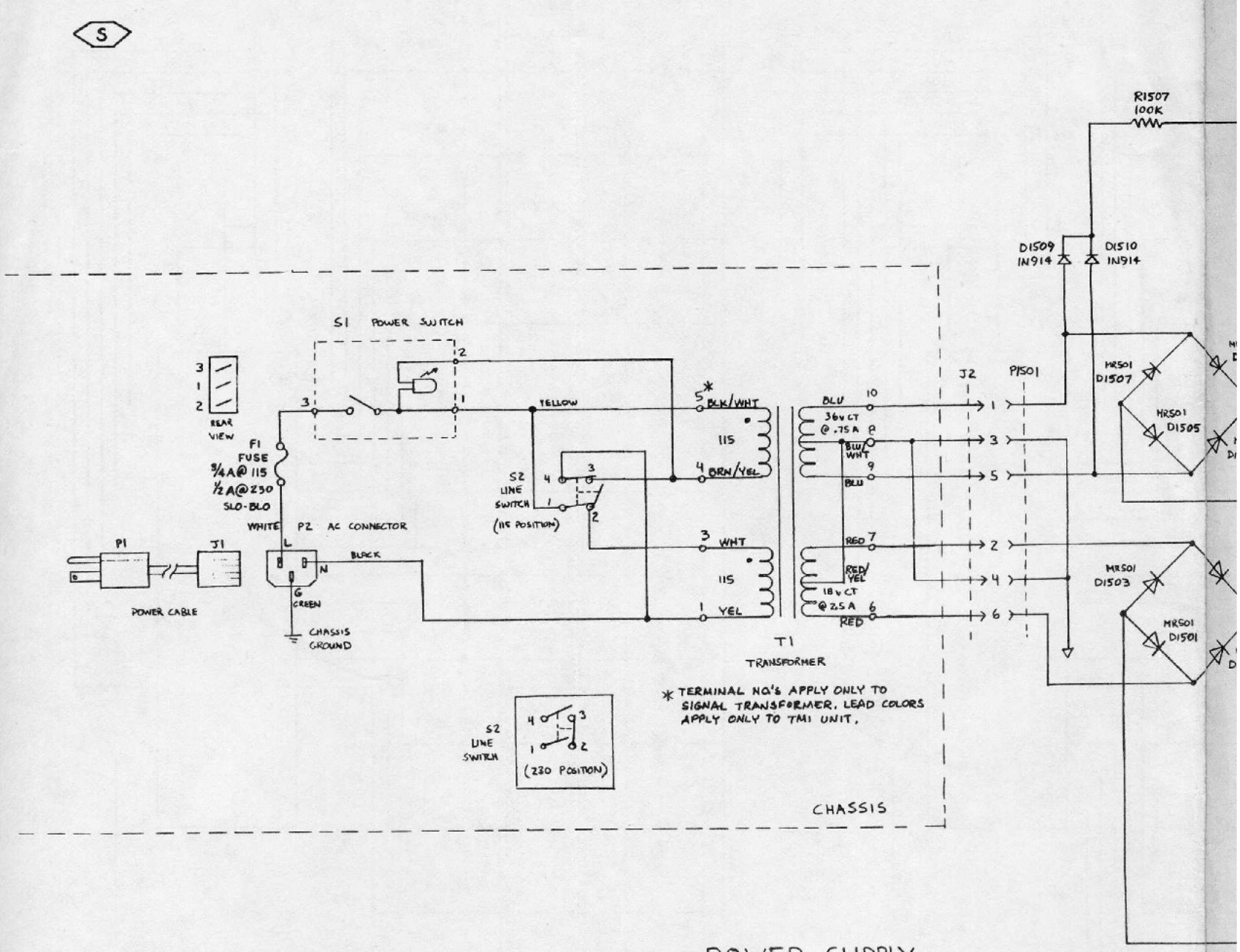
SCALE | SHEET 1 OF 1

DO NOT SCALE DRAWING

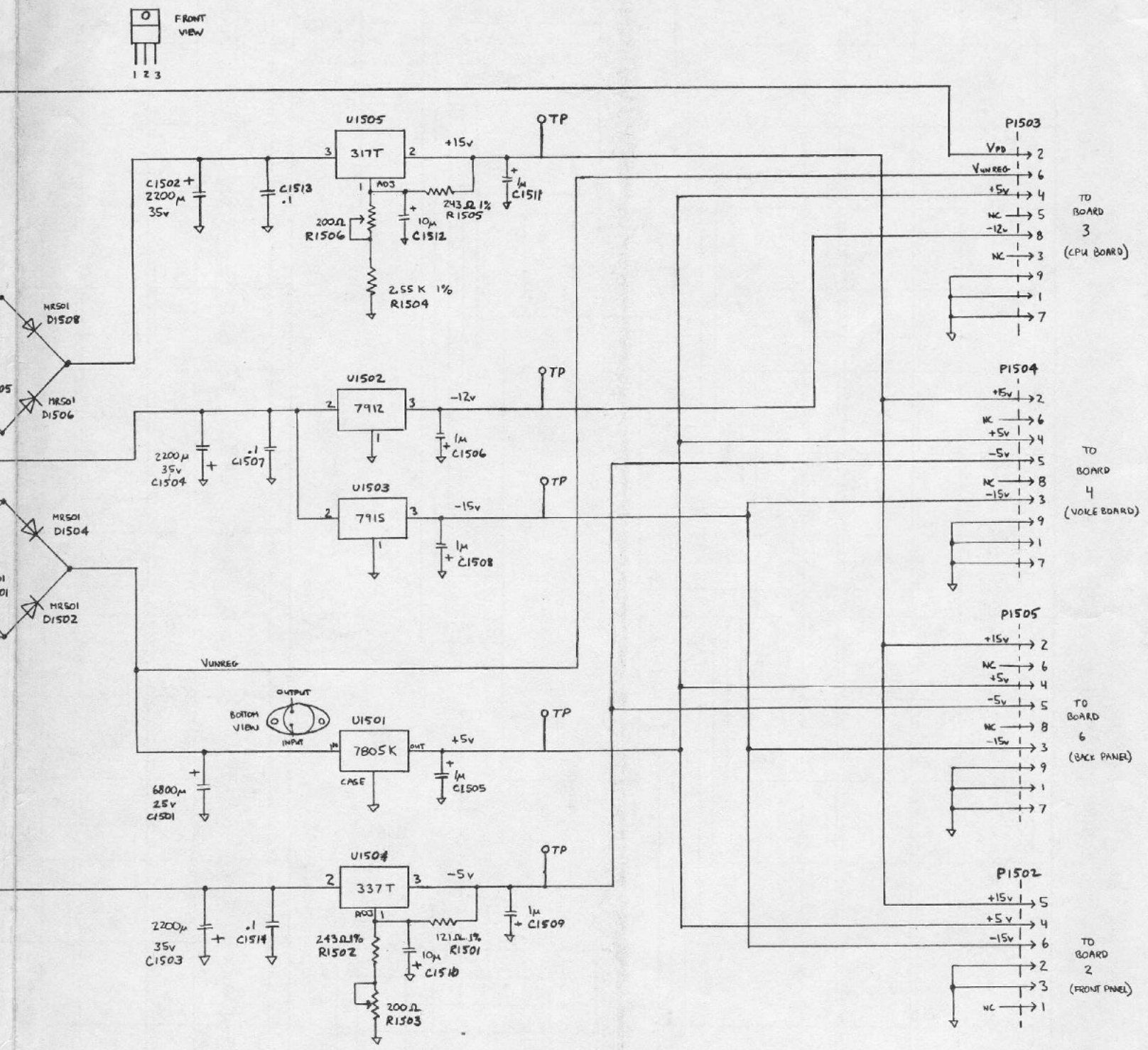

BOARD12
BOARD13
+5a
R
P
F3
F#3
G3
G#3
A3
A#3
B3
C4
C#4
D4
D#4
E4
F4
F#4
G4
G#4
RA1201
RA1202
10K (ALL)
C1202 2.2
C1203 2.2
C1204 2.2
C1205 2.2
C1206 2.2
C1207 2.2
C1208 2.2
C1209 2.2
C1210 2.2
C1211 2.2
C1212 2.2
C1213 2.2
C1214 2.2
C1215 2.2
C1216 2.2
C1217 2.2
PRESSURE SENSORS
TB1201
TB1202
VMUX
MUX D
MUX C
MUX A
C1201 .1
U1201
4067
Vdd
Vss
INO
IN15
A
B
C
D
I
R1201 1K
WIRE JUMPER
I3
I4
I5
I6
I7
A4
A#4
B4
C5
C#5
D5
D#5
E5
F5
F#5
G5
G#5
A5
A#5
B5
C6
RA1301
RA1302
C1302 2.2
C1303 2.2
C1304 2.2
C1305 2.2
C1306 2.2
C1307 2.2
C1308 2.2
C1309 2.2
C1310 2.2
C1311 2.2
C1312 2.2
C1313 2.2
C1314 2.2
C1315 2.2
C1316 2.2
C1317 2.2



								J	SEQUENTIAL CIRCUITS INC
								H	
								G	
								F	APPROVALS / DATE / TITLE: PRESSURE BOARDS
								E	DWN -A / 5/1/83
								D	CHK Dawn / 6/13/83 / SIZE: 1008
								C	DSN / DOCUMENT No.: SD008-12/13/14 / REV: B
			5-9-83			CHANGED JUMP DESIGNATORS		B	PEN / SCALE / SHEET 1 OF 1
DO NOT SCALE DRAWING			DATE			REVISION		A	ISS



POWER SUPPLY



LAST USED :
C1514
D1510
R1507
P1505
U1505

							J	
							H	
							G	
							F	
							E	
							D	
							C	
							B	
							A	
DO NOT SCALE DRAWING		DATE			REVISION		LTR	

SEQUENTIAL CIRCUITS INC

APPROVALS	DATE
DWN DAVE	1/6/82
CHK Dennis	6/13/82
DSN	
PEN	
ISS	

TITLE: BOARD 15 SCHEMATIC
SIZE: | MODEL No. 1008
DOCUMENT No. SD 1008-15 | REV B
SCALE — | SHEET 1 OF 1

T8 DIAGNOSTIC PROCEDURES

Notes: Because the normal operating software completely fills the Z80 PROM, a seperate PROM is required to run these tests. The Z8002 diagnostics reside in the normal system PROMs. The diagnostics described in this procedure cover most of the digital circuitry in the machine; if a problem has been localized to a general area in hardware, portions of this procedure may be skipped.

Z80 TESTS

Notes: Z80 tests are selected using program select buttons 1 through 5. The current test number is displayed on the right program LED display.

1. Install Z80 diagnostic PROM (DIAGT8) in IC22 socket.

2. Disable Z8002 by shorting BUSREQ test point to ground with a clip lead.

3. Power-up the machine. The Z80 is now in a loop waiting for a program select button to indicate the desired test. Execute tests 1 through 5.

4. Troubleshoot any test failures.

Z8002 TESTS

Notes: The diagnostic software is accessed by momentarily grounding the -NMI test point (short duration less than one second; this pin is debounced in software). The program advances to the next test routine each time the pin is shorted (allow 5 seconds for the next test to begin). Disconnect the audio monitor system from the T8 before running these tests.

1. Remove the ground clip from -BUSREQ if present. Disable the Z80 using the Z80 -BUSREQ pin.

2. Start test number 1 using -NMI.

3. When test two is correctly executing, remove the Z80 -BUSREQ ground clip and select test number 4 of the Z80 diagnostics. Z80 and Z8002 common ram tests are now running simultaneously, which is a 100% test of common ram circuitry. If both tests pass, disable the Z80 again and proceed with Z8002 tests 3-17.

4. Troubleshoot any test failures,

Z80 DIAGNOSTIC TEST DESCRIPTIONS

TEST 1: I/O PORT TEST

This test alternately writes 55H (01010101) and AAH (10101010) to all output ports. At the same time, all input ports are being read. This test verifies all chip-select decoding circuitry.

TEST 2: LED TEST

All LEDs on the front panel are lit in sequence.

TEST 3: RAM TEST

A memory test is performed on Scratch Pad RAM, Program RAM, and Sequencer RAM. This test is destructive so programs and sequences should be saved to tape before executing the test. The results of the test are displayed on the PROGRAM SELECT LEDs as follows:

PROG SEL LED 1 = U312 failed RAM test.
PROG SEL LED 2 = U316 failed RAM test.
PROG SEL LED 3 = U311 failed RAM test.
PROG SEL LED 4 = U313 failed RAM test.
PROG SEL LED 5 = U317 failed RAM test.

No LEDs on except test # indicates RAM test passed.

TEST 4: COMMON RAM TEST

A memory test is performed on the lower 1k address space of Common RAM. The results are displayed on the PROGRAM SELECT LEDs according to the following format:

PROG SEL LED 1 = U335 failed RAM test.
PROG SEL LED 2 = U337 failed RAM test.

No LEDs on except test # indicates RAM test passed.

TEST 5: POT AND PRESSURE SENSOR TEST

Performs ADC of all pots (except Master Volume and Balance), Pitch Wheel, Mod Wheel, and all pressure sensors. The 8 bit sum of all conversion results is displayed in hex on the right program display. With all pots initialized to zero, each pot can be rotated to check that it covers the full range from 00H to FFH. The pressure sensors are tested in the same way, although it is normal for some sensors to not quite reach FFH.

Z8002 DIAGNOSTIC TEST DESCRIPTIONS

TEST 1: uOUT TOGGLE

This test requires a minimal amount of hardware to pass. It verifies correct PROM access, data and address bus integrity, correct power supplies, and other minimum Z8002 operating conditions.

Pass is indicated by a continous pulse train on the uOUT tst point.

TEST 2: COMMON RAM

This test checks the top half of common ram and associated arbitration logic. It may be run simultaneously with the Z80 common ram test, which accesses the lower half of common ram. In operation, the test writes the upper 1k of ram with a sequence of numbers. The sequence is then read and checked for errors. This cycle will continue to repeat unless an error is found.

Pass is indicated by a continuous train of widely-spaced pulses. The fail loop produces a high-frequency square wave.

TEST 3: DAC TEST

This test verifies interrupt, FIFO, and DAC hardware. An ascending sequence of numbers is repeatedly output to the FIFO, resulting in a ramp waveform at the DAC output buffer. All bits are used, and any hardware problems affecting the data will appear as nonlinearity in the ramp waveform. Problems with the low order bits may not be visible; these bits can be checked with tests 4-17.

TESTS 4-17: BIT TESTS

Each of these tests outputs a constant value to the DAC, which will appear on all sample holds. Starting with the DAC MSB, there is only one bit set per test. As tests are advanced, each bit value can be measured with a DVM if desired.

Note: Shorting -NMI after the last bit test will initiate test number 1. To execute the normal operating software, the power must be switched off.